CYM1420

128K x 8 Static RAM Module

Features

- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 20 ns**
- **32-pin, 0.6-inch-wide DIP package**
- **Low active power**
  - **1.2W (max.)**
- **FR4 SMD technology**
- **TTL-compatible inputs and outputs**
- **JEDEC-compatible pinout**
- **Commercial temperature range**

Functional Description

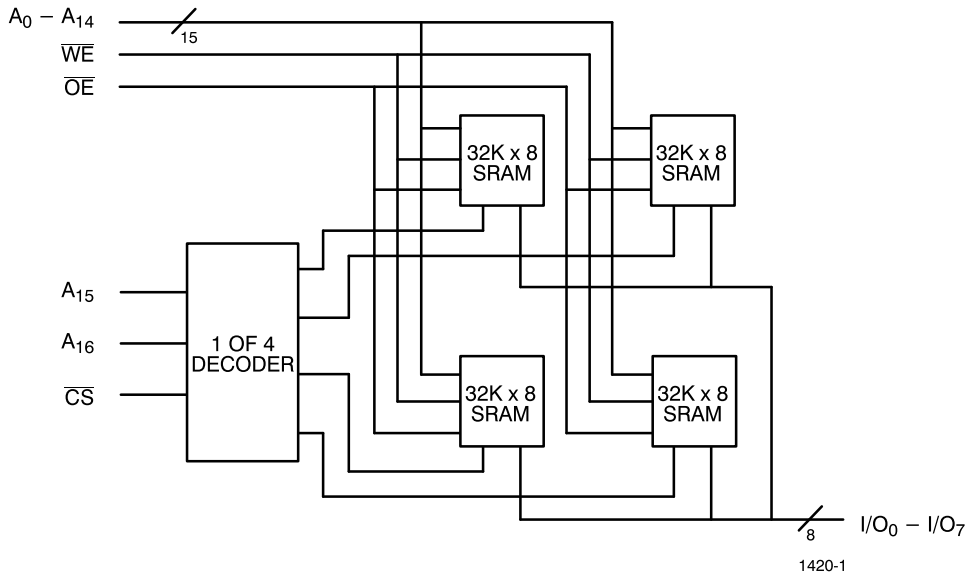
The CYM1420 is a very high performance 1-megabit static RAM module organized as 128K words by 8 bits. This module is constructed using four 32K x 8 static RAMs mounted onto a substrate. A decoder is used to interpret the higher-order addresses A_{15} and A_{16} and to select one of the four RAMs.

Writing to the memory module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight input/output pins (I/O_0 through I/O_7) of the device is written into the memory location specified on the address pins (A_0 through A_{16}).

Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the eight input/output pins.

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram



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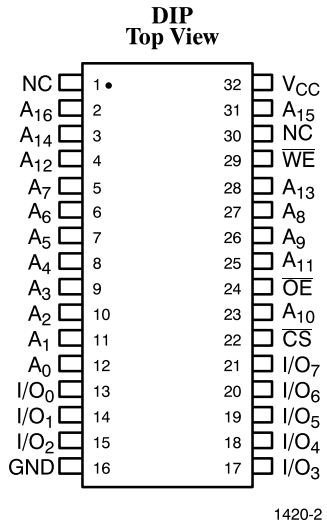
Pin Configuration



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Selection Guide

		1420–20	1420–25	1420–30	1420–35	1420–45	1420–55
Maximum Access Time (ns)		20	25	30	35	45	55
Maximum Operating Current (mA)	Commercial	210	210	210	210	210	210
Maximum Standby Current (mA)	Commercial	140	140	140	140	140	140

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with .. − 10°C to +85°C (Commercial)

Supply Voltage to Ground Potential ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

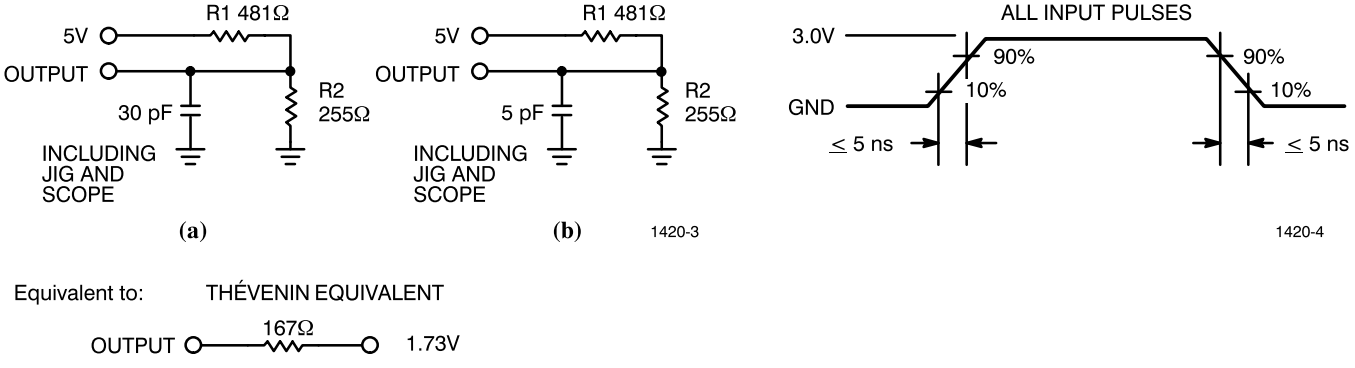
Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	− 10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	− 10	+10	μA
I_{OS}	Output Short Circuit Current[1, 2]	V_{CC} = Max., V_{OUT} = GND		− 300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		210	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[3]	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		140	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[3]	V_{CC} = Max., $\overline{CS}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V		80	mA

Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	35	pF
C_{OUT}	Output Capacitance		40	pF

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. Tested on a sample basis.
3. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.

Switching Characteristics Over the Operating Range[4]

Parameters	Description	1420−20		1420−25		1420−30		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	20		25		30		ns
t_{AA}	Address to Data Valid		20		25		30	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		20		25		30	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		10		15	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		10		10		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[5]	3		3		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[5, 6]		20		20		20	ns
WRITE CYCLE[7]								
t_{WC}	Write Cycle Time	20		25		30		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	15		20		25		ns
t_{AW}	Address Set-Up to Write End	15		20		25		ns
t_{HA}	Address Hold from Write End	2		2		5		ns
t_{SA}	Address Set-Up to Write Start	5		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		20		25		ns
t_{SD}	Data Set-Up to Write End	10		12		18		ns
t_{HD}	Data Hold from Write End	2		2		3		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]	0	8	0	10	0	15	ns

Notes:

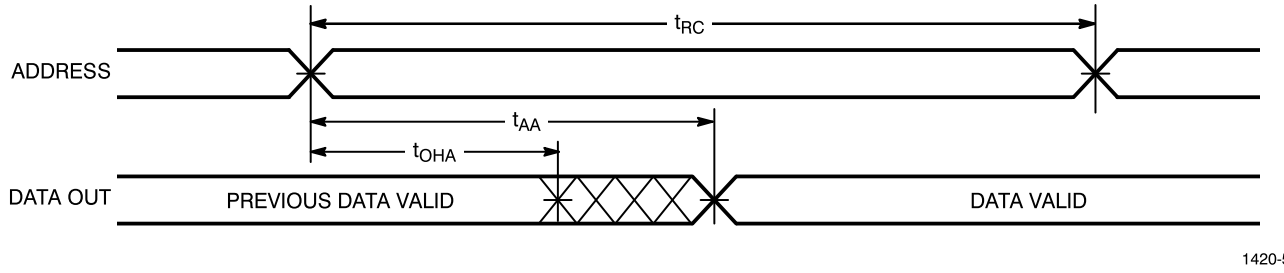
4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
6. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics Over the Operating Range (continued)[4]

Parameters	Description	1420−35		1420−45		1420−55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid		35		45		55	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		18		25		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		20		20		25	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[5]	3		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[5, 6]		20		20		25	ns
WRITE CYCLE[7]								
t_{WC}	Write Cycle Time	35		45		55		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	30		40		45		ns
t_{AW}	Address Set-Up to Write End	30		40		45		ns
t_{HA}	Address Hold from Write End	5		5		5		ns
t_{SA}	Address Set-Up to Write Start	5		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	25		25		30		ns
t_{SD}	Data Set-Up to Write End	18		20		25		ns
t_{HD}	Data Hold from Write End	3		5		5		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]	0	15	0	15	0	25	ns

Switching Waveforms

Read Cycle No. 1[8, 9]



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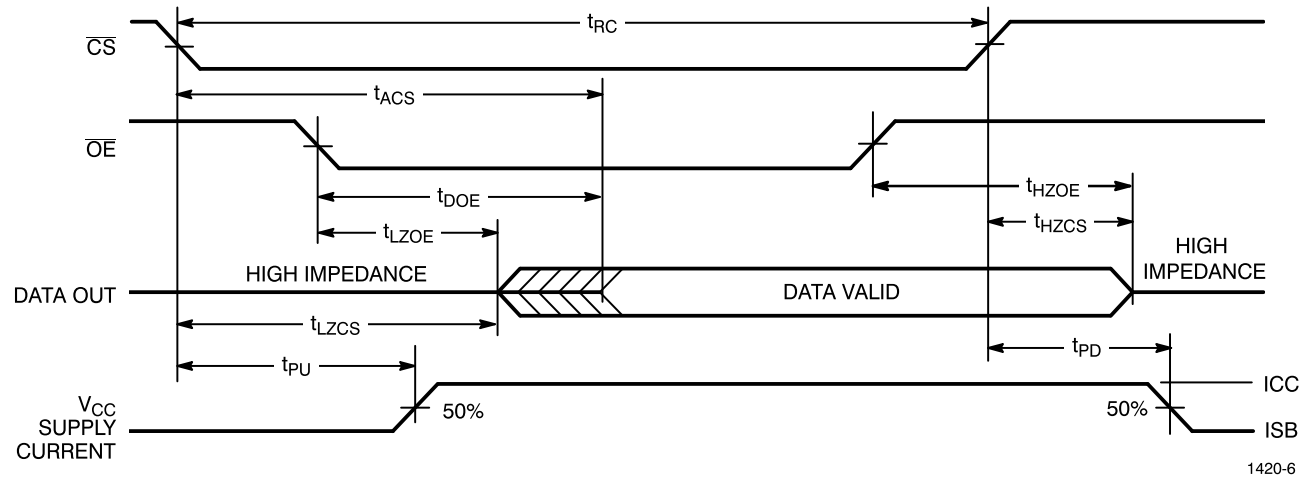
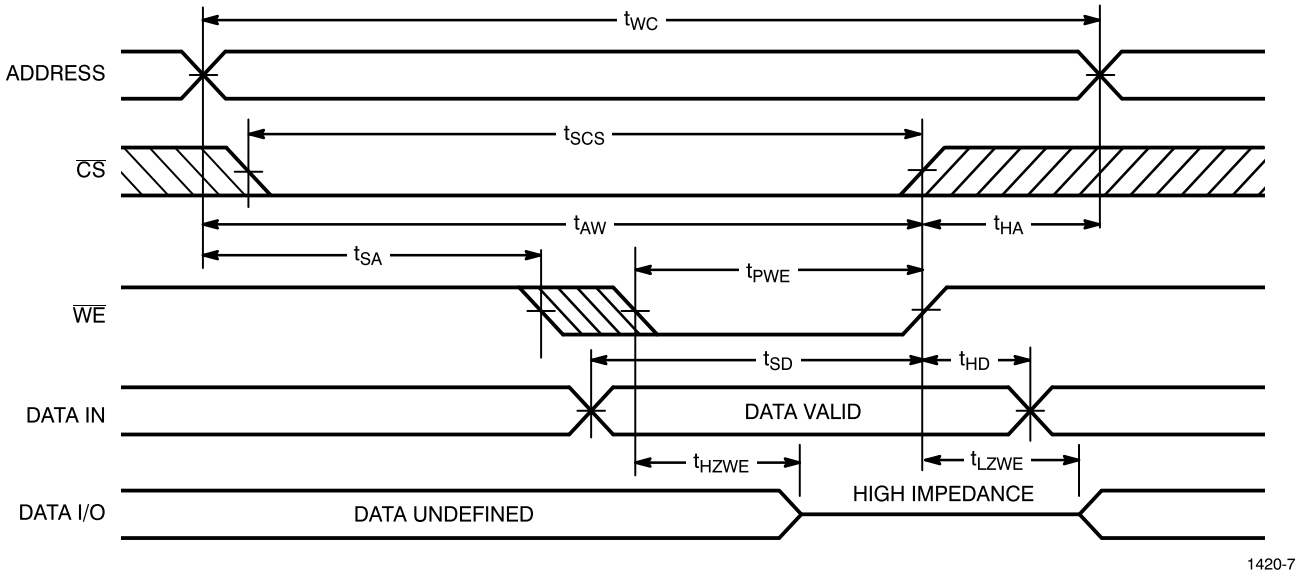
Notes:
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{OE}$= V_{IL}.

Switching Waveforms (continued)

Read Cycle No. 2[8, 10]



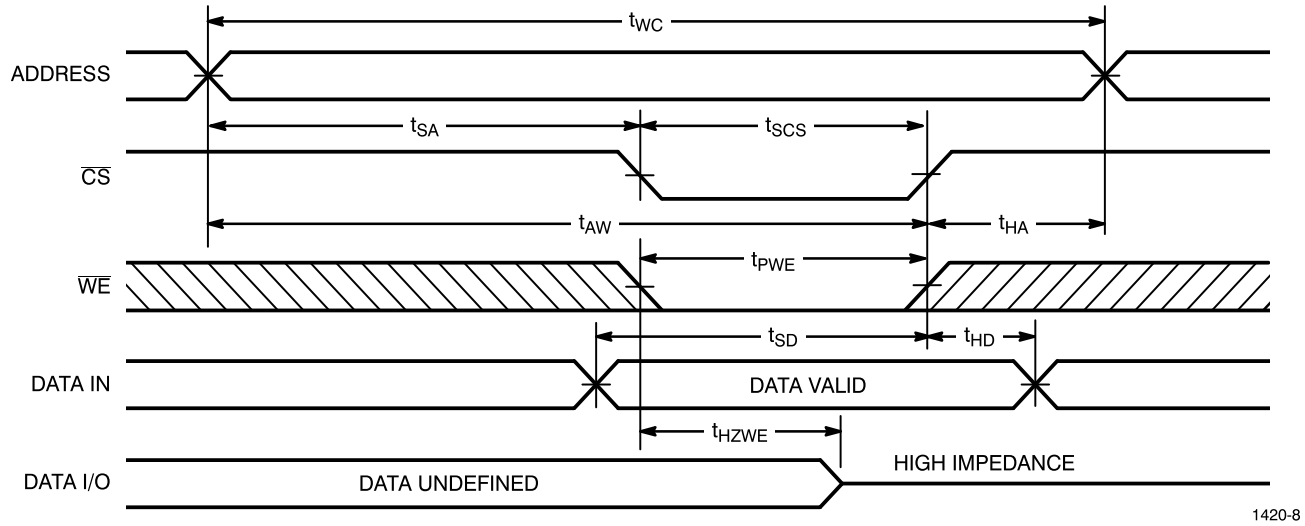
Write Cycle No. 1 ($\overline{WE}$ Controlled)[7, 11]



Notes:
10. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
11. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[7, 11, 12]



Note:
12. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Inputs/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	L	H	Data Out	Read
L	X	L	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CYM1420PD−20C	PD05	32-Pin DIP Module	Commercial
25	CYM1420PD−25C	PD05	32-Pin DIP Module	Commercial
30	CYM1420PD−30C	PD05	32-Pin DIP Module	Commercial
35	CYM1420PD−35C	PD05	32-Pin DIP Module	Commercial
45	CYM1420PD−45C	PD05	32-Pin DIP Module	Commercial
55	CYM1420PD−55C	PD05	32-Pin DIP Module	Commercial

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Package Diagrams

32-Pin DIP Module PD05