CYM1464

512K x 8 Static RAM Module

Features

- **High-density 4-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 20 ns**
- **Low active power**
  - **1.93W (max.)**
- **JEDEC-compatible pinout**
- **32-pin, 0.6-inch-wide DIP package**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of 0.34 inches**

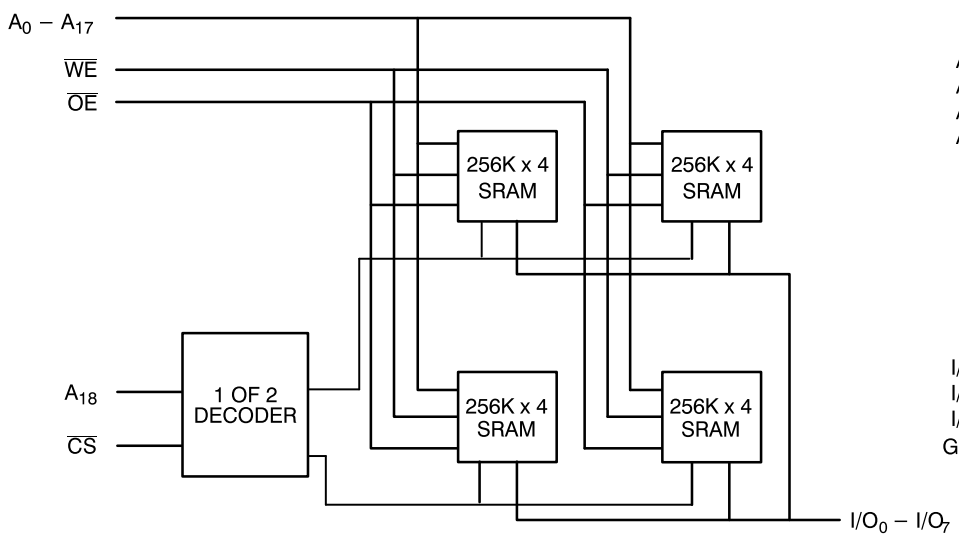
Functional Description

The CYM1464 is a high-performance 4-megabit static RAM module organized as 512K words by 8 bits. This module is constructed using four 256K x 4 static RAMs in SOJ packages mounted on an epoxy laminate substrate with pins.

Writing to the module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight input/output pins (I/O_0 through I/O_7) of the device is written into the memory location specified on the address pins (A_0 through A_{18}). Reading the device is accomplished by taking chip select and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{18}) will appear on the eight appropriate data input/output pins (I/O_0 through I/O_7).

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram



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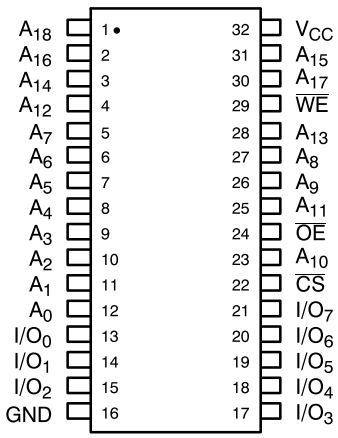
Pin Configuration

DIP
Top View



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Selection Guide

	1464–20	1464–22	1464–25	1464–30	1464–35	1464–45	1464–55
Maximum Access Time (ns)	20	22	25	30	35	45	55
Maximum Operating Current (mA)	350	350	350	300	300	300	300
Maximum Standby Current (mA)	240	240	240	240	240	240	240

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... −55°C to +125°C

Ambient Temperature with Power Applied ..... −10°C to +85°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	1464−20, 22, 25		1464−30, 35, 45, 55		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]		−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_0 ≤ V_{CC}, Output Disabled	−10	+10	−10	+10	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		350		300	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		240		240	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current	V_{CC} = Max., $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V		60		60	mA

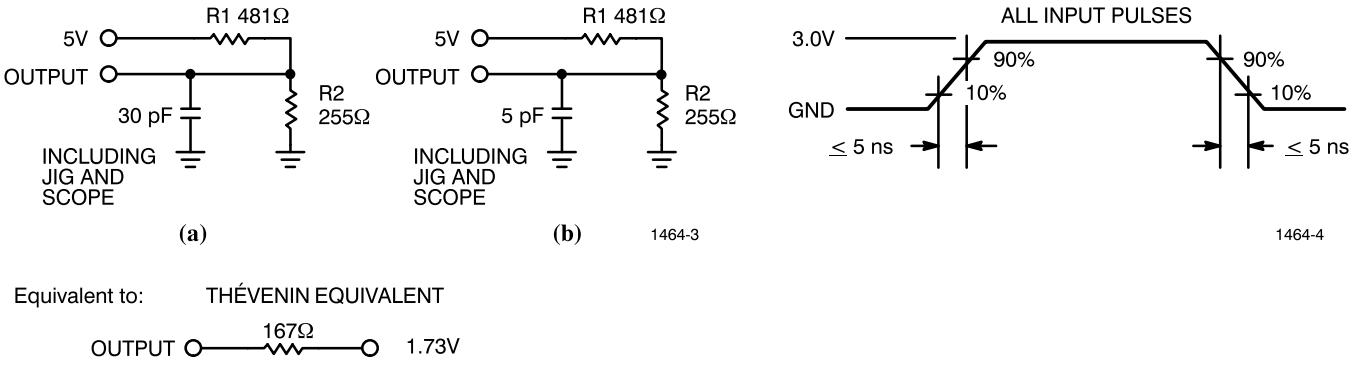
Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	40	pF
C_{OUT}	Output Capacitance		30	pF

Notes:

1. V_{IL} (min.) = −3.0V for pulse widths less than 20 ns.
2. Tested on a sample basis.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

Switching Characteristics Over the Operating Range[3]

Parameter	Description	1464−20		1464−22		1464−25		1464−30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	20		22		25		30		ns
t_{AA}	Address to Data Valid		20		22		25		30	ns
t_{OHA}	Data Hold from Address Change	5		5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		20		22		25		30	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		13		13		15		15	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z	0	10	0	10	0	10	0	10	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z	5		5		5		10		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4]	0	15	0	15	0	15	0	20	ns
WRITE CYCLE[5]										
t_{WC}	Write Cycle Time	20		22		25		30		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	15		17		20		25		ns
t_{AW}	Address Set-Up to Write End	15		15		20		25		ns
t_{HA}	Address Hold from Write End	3		3		3		3		ns
t_{SA}	Address Set-Up to Write Start	5		5		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		15		15		20		ns
t_{SD}	Data Set-Up to Write End	12		12		15		15		ns
t_{HD}	Data Hold from Write End	2		2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[4]		15		15		15		15	ns

Notes:

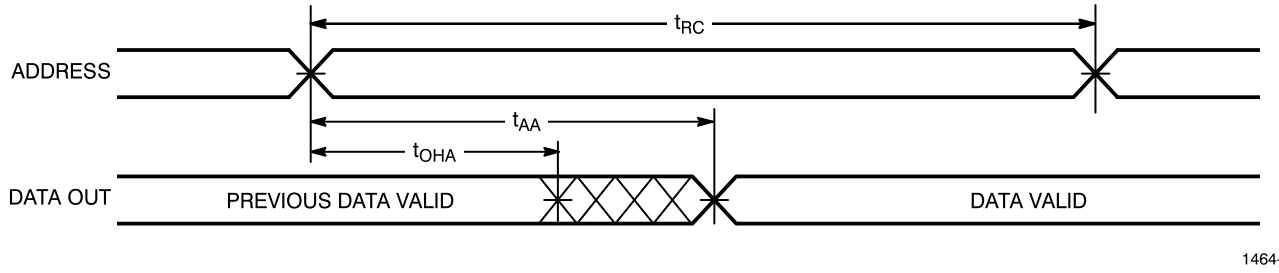
3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. t_{HZCS} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
5. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics Over the Operating Range (continued)[3]

Parameter	Description	1464−35		1464−45		1464−55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid		35		45		55	ns
t_{OHA}	Data Hold from Address Change	5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		20		25		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z	0	15	0	15	0	15	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z	10		10		10		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4]	0	20	0	20	0	20	ns
WRITE CYCLE[5]								
t_{WC}	Write Cycle Time	35		45		55		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	30		40		50		ns
t_{AW}	Address Set-Up to Write End	30		40		50		ns
t_{HA}	Address Hold from Write End	3		3		3		ns
t_{SA}	Address Set-Up to Write Start	6		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	25		35		40		ns
t_{SD}	Data Set-Up to Write End	20		25		35		ns
t_{HD}	Data Hold from Write End	2		3		3		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[4]		15		15		20	ns

Switching Waveforms

Read Cycle No. 1[6, 7]



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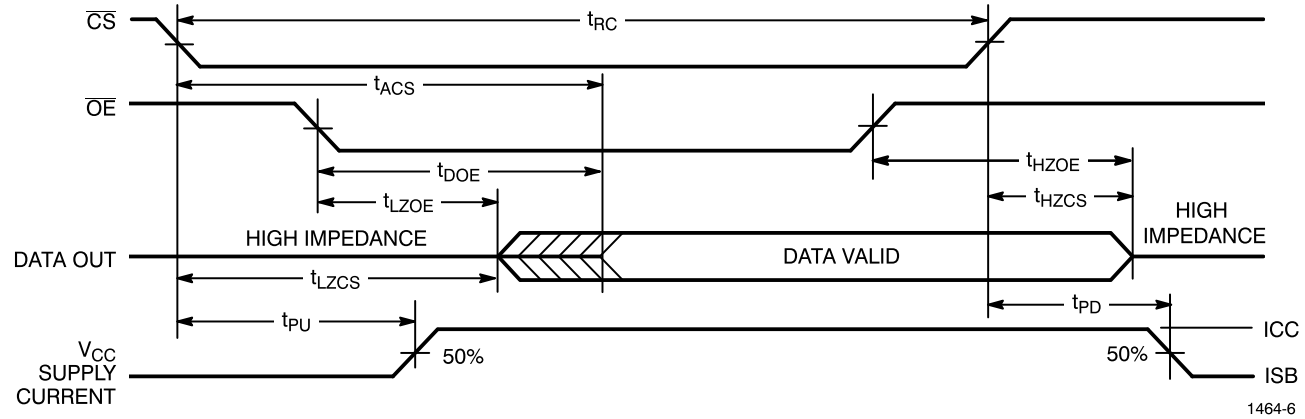
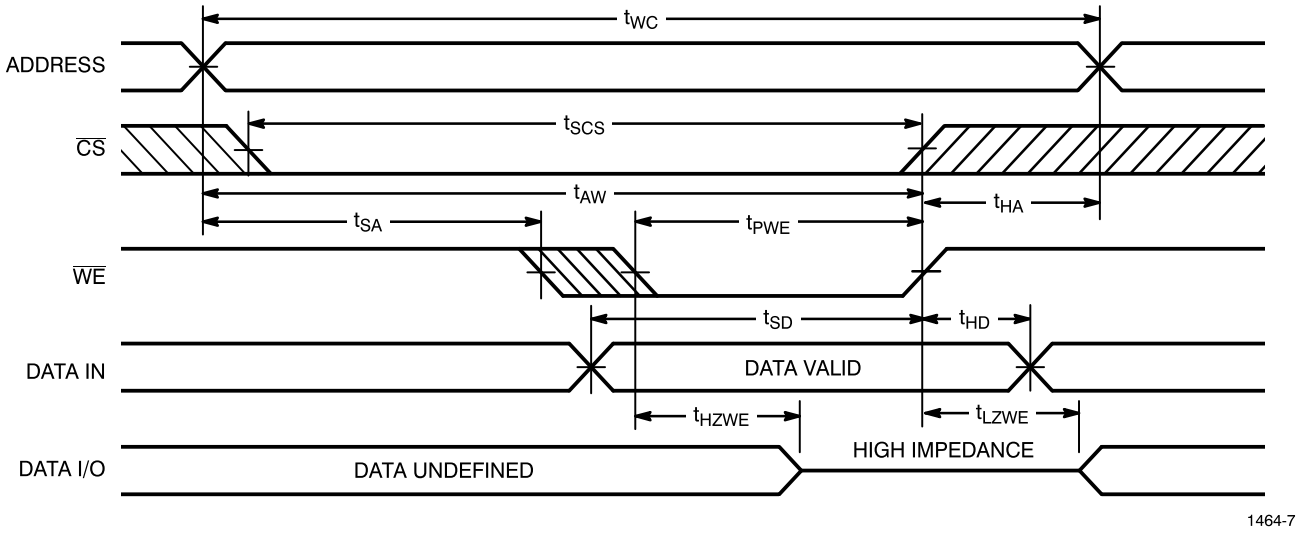
Notes:
6. $\overline{WE}$ is HIGH for read cycle.
7. Device is continuously selected, $\overline{CS}$ = V_{IL}.

Switching Waveforms (continued)

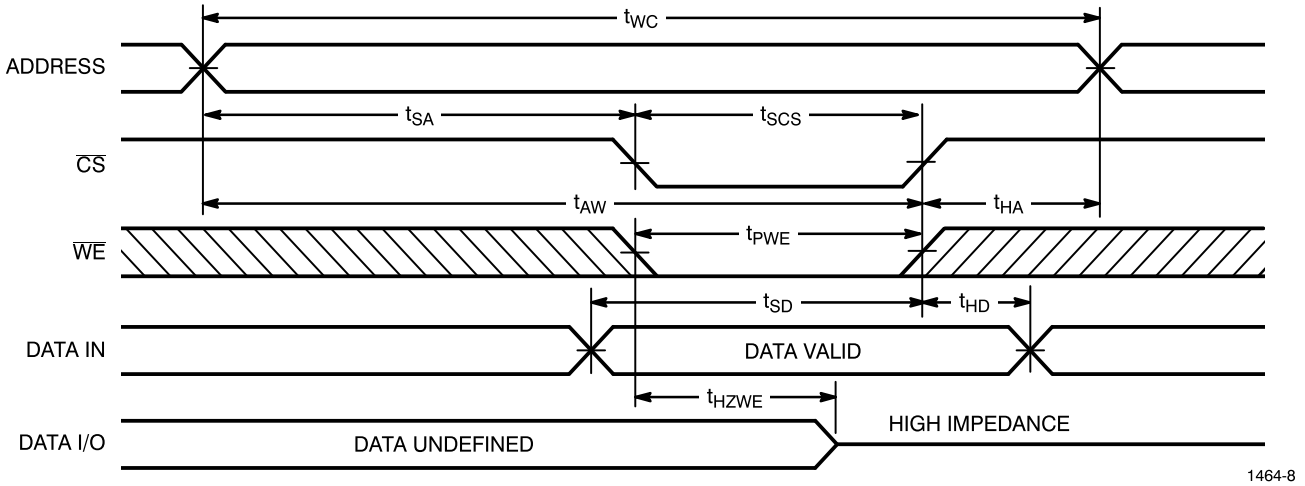
Read Cycle No. 2[6, 8]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[5]



Write Cycle No. 2 ($\overline{CS}$ Controlled)[5, 9]



Notes:
8. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
9. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read Word
L	L	X	Data In	Write Word
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
20	CYM1464PD−20C	PD02	32-Pin DIP Module	Commercial
22	CYM1464PD−22C	PD02	32-Pin DIP Module	Commercial
25	CYM1464PD−25C	PD02	32-Pin DIP Module	Commercial
30	CYM1464PD−30C	PD02	32-Pin DIP Module	Commercial
35	CYM1464PD−35C	PD02	32-Pin DIP Module	Commercial
45	CYM1464PD−45C	PD02	32-Pin DIP Module	Commercial
55	CYM1464PD−55C	PD02	32-Pin DIP Module	Commercial

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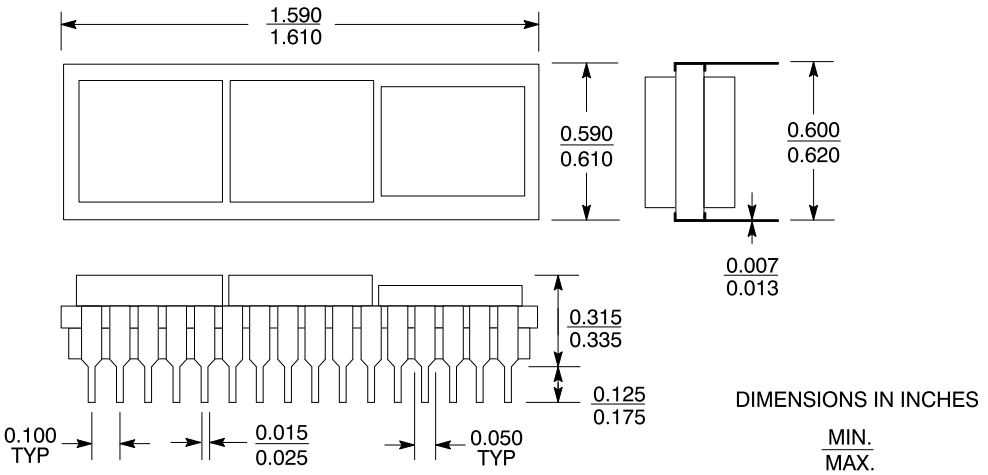
Package Diagrams

32-Pin DIP Module PD02



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