CYM1465

512K x 8 SRAM Module

Features

- **High-density 4-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 70 ns**
- **Low active power**
  - **605 mW (max.)**
- **2V data retention (L Version)**
- **JEDEC-compatible pinout**
- **32-pin, 0.6-inch-wide DIP package**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of 0.27 in.**
- **Small PCB footprint**
  - **0.98 sq. in.**

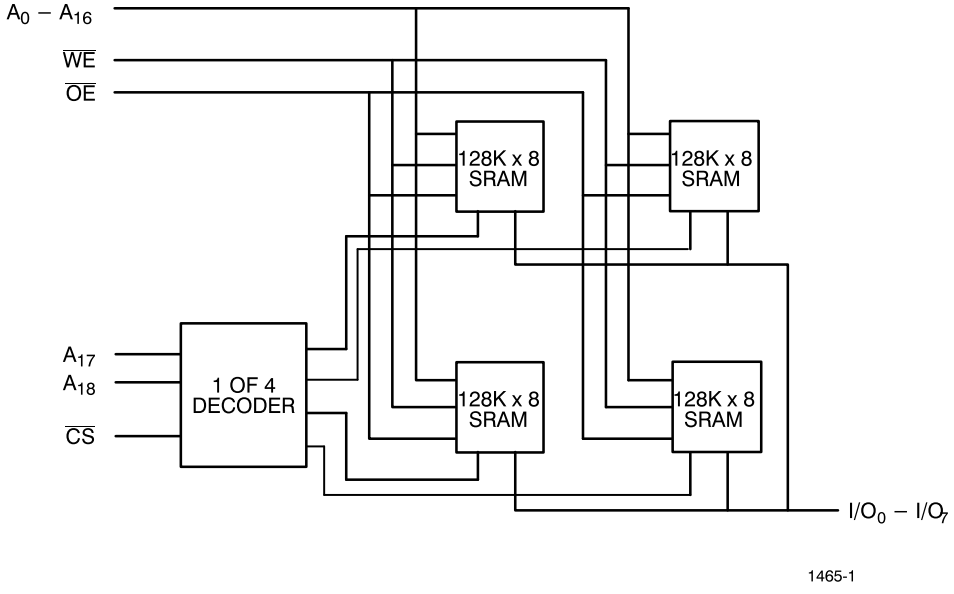
Functional Description

The CYM1465 is a high-performance 4-megabit static RAM module organized as 512K words by 8 bits. This module is constructed using four 128K x 8 RAMs mounted on a substrate with pins. A decoder is used to interpret the higher-order addresses (A_{17} and A_{18}) and to select one of the four RAMs.

Writing to the module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight input/output pins (I/O_0 through I/O_7) of the device is written into the memory location specified on the address pins (A_0 through A_{18}). Reading the device is accomplished by taking chip select and output enable ($\overline{OE}$) LOW while write enable remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{18}) will appear on the eight appropriate data input/output pins (I/O_0 through I/O_7).

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable is HIGH.

Logic Block Diagram



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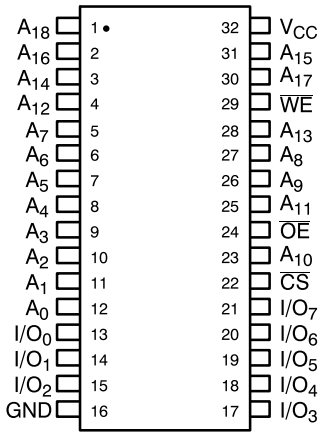
Pin Configuration

DIP
Top View



1465-2

Selection Guide

	1465–70	1465–85	1465–100	1465–120	1465–150
Maximum Access Time (ns)	70	85	100	120	150
Maximum Operating Current (mA)	110	110	110	110	110
Maximum Standby Current (mA)	12	12	12	12	12

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... −55°C to +150°C

Ambient Temperature with Power Applied ..... −10°C to +85°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%

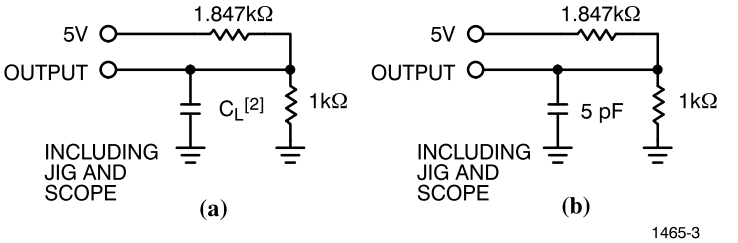
Electrical Characteristics Over the Operating Range

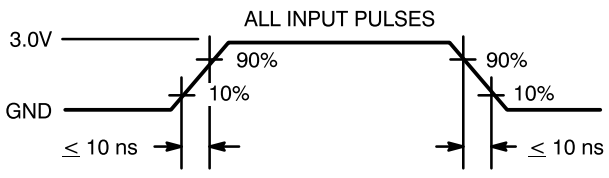
Parameter	Description	Test Conditions		1465 Min.	1465 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 1.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.1 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage			−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−20	+20	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}			110	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%			12	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V	Standard Version		8	mA
			L Version		420	µA

Capacitance[1]

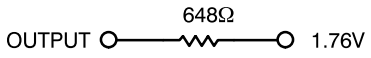
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	45	pF
C_{OUT}	Output Capacitance		45	pF

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Notes:

1. Tested on a sample basis.
2. Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance for 85-, 100-, 120-, and 150-ns speeds. C_L = 30 pF for 70-ns speed.

Switching Characteristics Over the Operating Range[2]

Parameter	Description	1465−70		1465−85		1465−100		1465−120		1465−150		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	70		85		100		120		150		ns
t_{AA}	Address to Data Valid		70		85		100		120		150	ns
t_{OHA}	Data Hold from Address Change	10		10		10		10		10		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		70		85		100		120		150	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		35		45		50		60		75	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	5		5		5		5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[3]		25		30		35		45		55	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z	10		10		10		10		10		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[3]		30		30		35		45		60	ns
WRITE CYCLE[4]												
t_{WC}	Write Cycle Time	70		85		100		120		150		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	65		75		90		100		115		ns
t_{AW}	Address Set-Up to Write End	65		75		90		100		110		ns
t_{HA}	Address Hold from Write End	0		5		5		5		5		ns
t_{SA}	Address Set-Up to Write Start	0		5		5		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	55		65		75		85		95		ns
t_{SD}	Data Set-Up to Write End	30		35		40		45		50		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[3]		25		30		35		40		45	ns

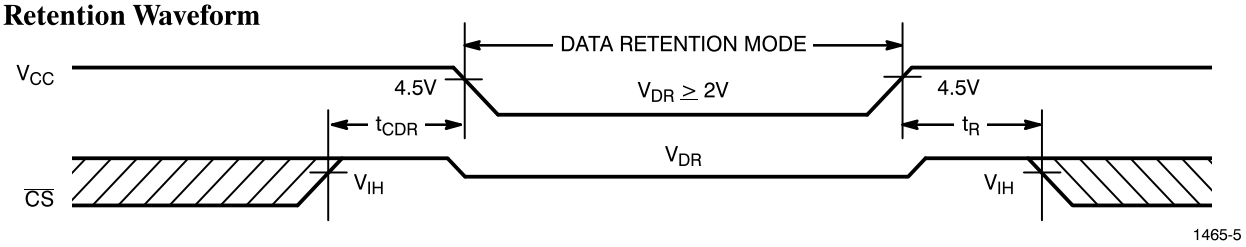
Data Retention Characteristics Over the Operating Range (L Version Only)

Parameter	Description	Test Conditions	Commercial		Industrial		Unit
			Min.	Max.	Min.	Max.	
V_{DR}	V_{CC} for Retention Data	$\overline{CS} \geq V_{CC} - 0.2V$	2		2		V
I_{CCDR3}	Data Retention Current	$V_{DR} = 3.0V$, $\overline{CS} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		50		150	µA
t_{CDR}[5]	Chip Deselect to Data Retention Time		0		0		ns
t_R[5]	Operation Recovery Time		5		5		ms

Notes:

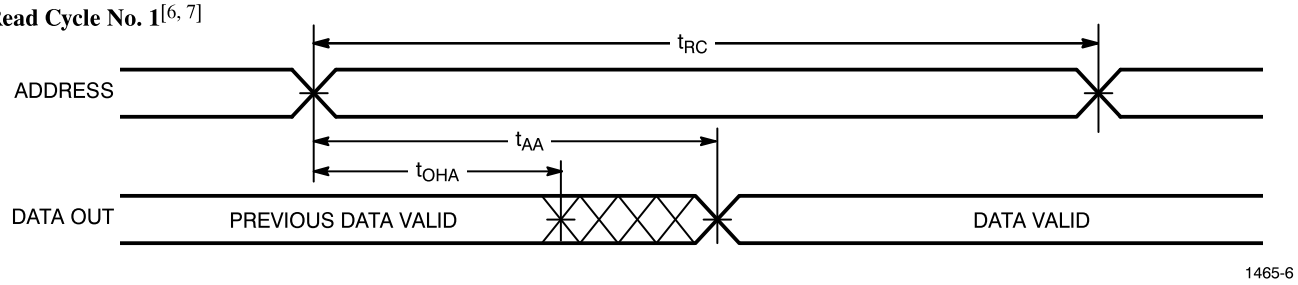
3. C_L = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
4. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
5. Guaranteed, not tested.

Data Retention Waveform

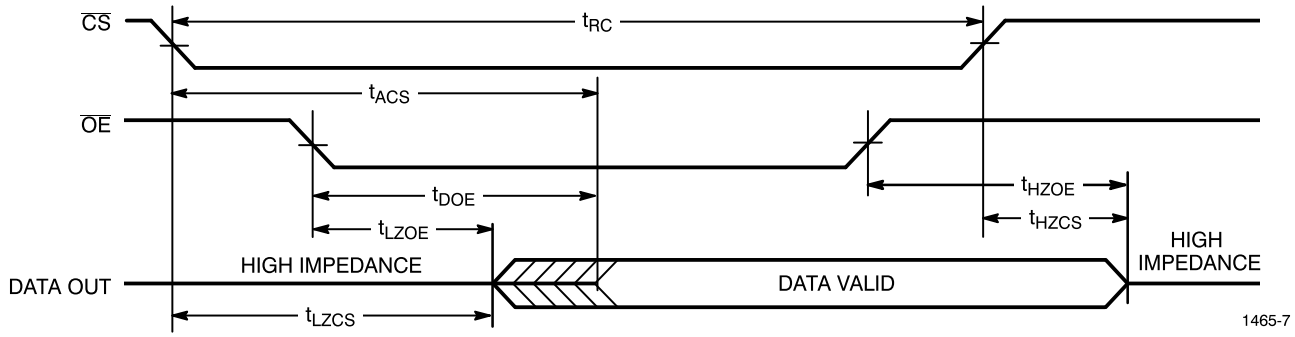


Switching Waveforms

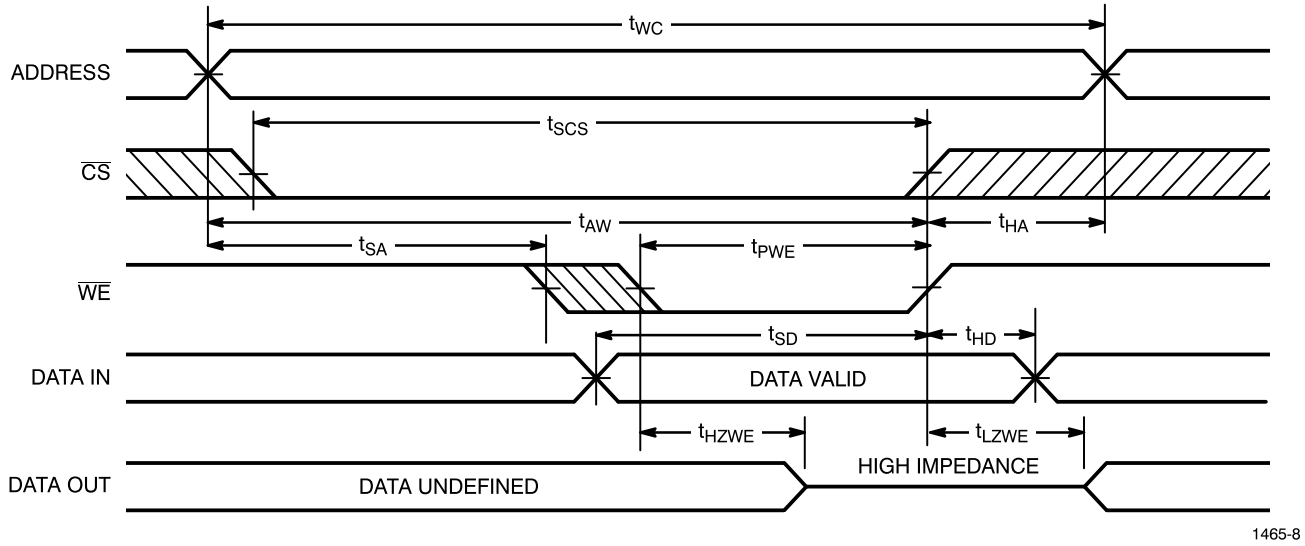
Read Cycle No. 1[6, 7]



Read Cycle No. 2[6, 8]



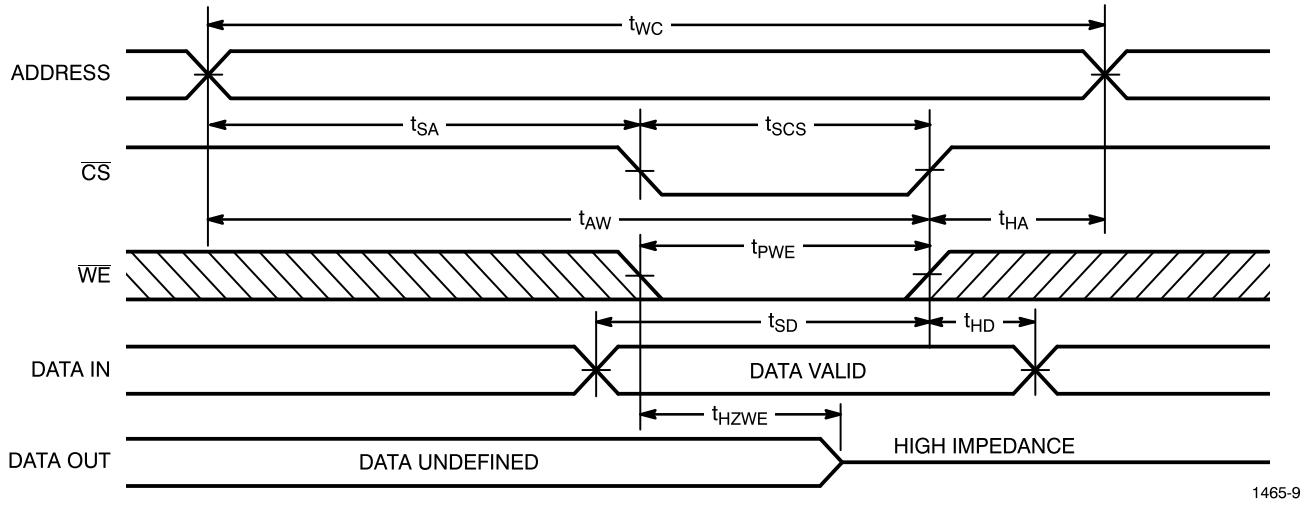
Write Cycle No. 1 ($\overline{WE}$ Controlled)[4]



Notes:
6. $\overline{WE}$ is HIGH for read cycle.
7. Device is continuously selected, $\overline{CS}$ = V_{IL}.
8. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[4, 9]



Note:
9. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

Inputs			Output	Mode
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$		
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read Word
L	L	X	Data In	Write Word
L	H	H	High Z	Deselect

CYM1465

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CYM1465PD−70C	PD03	32-Pin DIP Module	Commercial
	CYM1465LPD−70C			
85	CYM1465PD−85C	PD03	32-Pin DIP Module	Commercial
	CYM1465LPD−85C			
	CYM1465PD−85I	PD03	32-Pin DIP Module	Industrial
	CYM1465LPD−85I			
100	CYM1465PD−100C	PD03	32-Pin DIP Module	Commercial
	CYM1465LPD−100C			
	CYM1465PD−100I	PD03	32-Pin DIP Module	Industrial
	CYM1465LPD−100I			
120	CYM1465PD−120C	PD03	32-Pin DIP Module	Commercial
	CYM1465LPD−120C			
	CYM1465PD−120I	PD03	32-Pin DIP Module	Industrial
	CYM1465LPD−120I			
150	CYM1465PD−150C	PD03	32-Pin DIP Module	Commercial
	CYM1465LPD−150C			
	CYM1465PD−150I	PD03	32-Pin DIP Module	Industrial
	CYM1465LPD−150I			

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Package Diagrams

32-Pin DIP Module PD03