CYM1622

64K x 16 Static RAM Module

Features

- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **— Access time of 15 ns**
- **Low active power**
  - **— 2.2W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Pinout compatible with CYM1611**
- **Low profile**
  - **— Max. height of .50 in.**
- **Small PCB footprint**
  - **— 0.68 sq. in.**

Functional Description

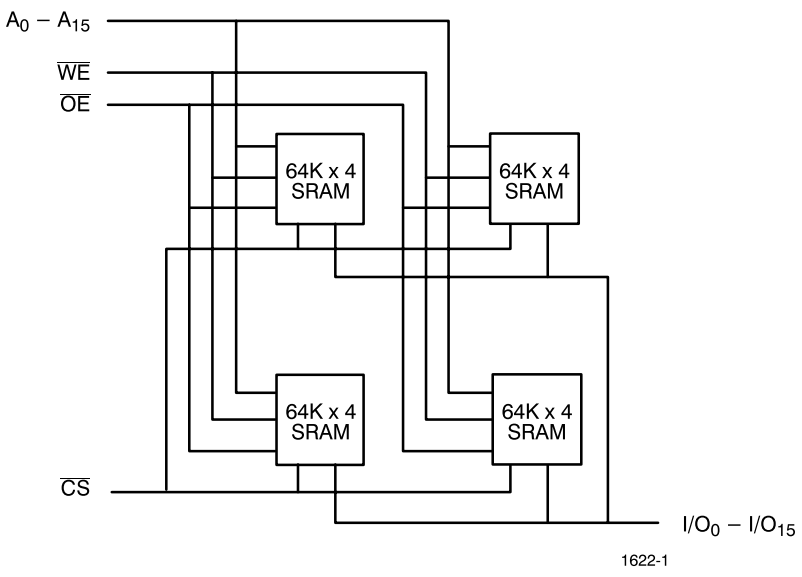
The CYM1622 is a very high performance 1-megabit static RAM module organized as 64K words by 16 bits. The module is constructed using four 64K x 4 static RAMs mounted onto a vertical substrate with pins. The pinout of this module is compatible with another Cypress module (CYM1611) to maximize system flexibility.

Writing to the memory module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the sixteen input/output pins (I/O_0 through I/O_{15}) of the device is written into the memory location specified on the address pins (A_0 through A_{15}).

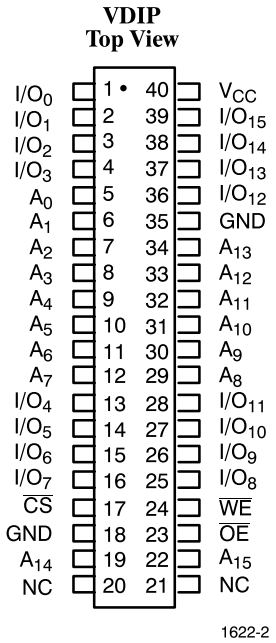
Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the appropriate data input/output pins.

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram



Pin Configuration



Selection Guide

	1622–15	1622–20	1622–25	1622–30	1622–35	1622–45
Maximum Access Time (ns)	15	20	25	30	35	45
Maximum Operating Current (mA)	600	500	400	400	400	400
Maximum Standby Current (mA)	80	80	140	140	140	140

Shaded areas contain preliminary information.

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... −65°C to +125°C

Ambient Temperature with Power Applied ..... −10°C to +80°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	1622−15		1622−20		1622−25, 30, 35, 45		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]		−0.5	0.8	−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−20	+20	−20	+20	−20	+20	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−10	+10	−10	+10	−10	+10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		600		500		400	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		160		160		140	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current	V_{CC} = Max., $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V		80		80		80	mA

Shaded areas contain preliminary information.

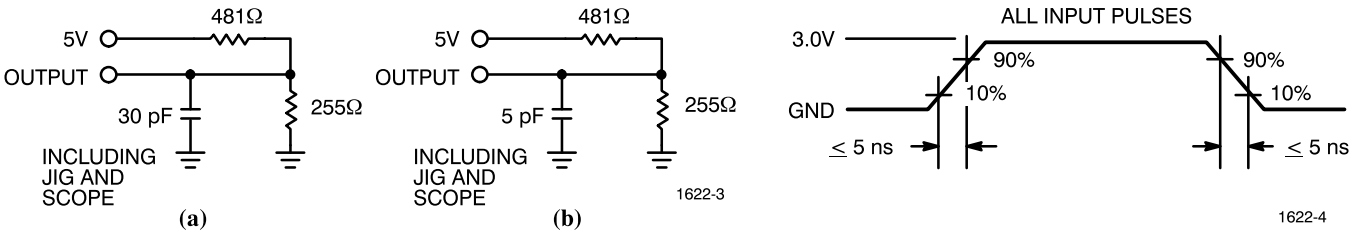
Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	35	pF
C_{OUT}	Output Capacitance		15	pF

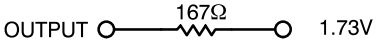
Notes:

1. V_{IL}(min.) = −3.0V for pulse widths less than 20 ns.
2. Tested on a sample basis.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3]

Parameter	Description	1622−15		1622−20		1622−25		1622−30		1622−35		1622−45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t_{RC}	Read Cycle Time	15		20		25		30		35		45		ns
t_{AA}	Address to Data Valid		15		20		25		30		35		45	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		15		20		25		30		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		8		10		15		20		25		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		8		10		15		20		20		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z	0		0		3		3		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4]		6		8		15		20		20		20	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0	25	0	30	0	35	0	45	ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		15		20		25		30		35		45	ns
WRITE CYCLE[5]														
t_{WC}	Write Cycle Time	15		20		25		30		35		45		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	10		15		20		25		30		40		ns
t_{AW}	Address Set-Up to Write End	10		15		20		25		30		40		ns
t_{HA}	Address Hold from Write End	2		2		3		3		3		3		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		15		20		25		25		30		ns
t_{SD}	Data Set-Up to Write End	8		12		15		20		20		25		ns
t_{HD}	Data Hold from Write End	2		2		2		2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[4]	0	7	0	10	0	15	0	15	0	15	0	20	ns

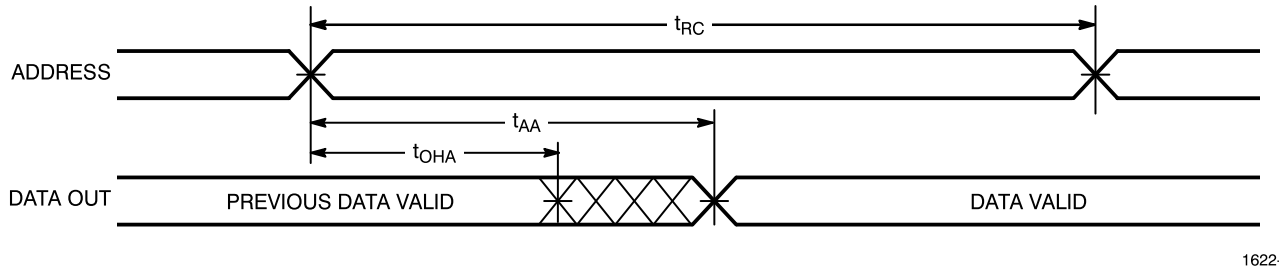
Shaded areas contain preliminary information.

Notes:

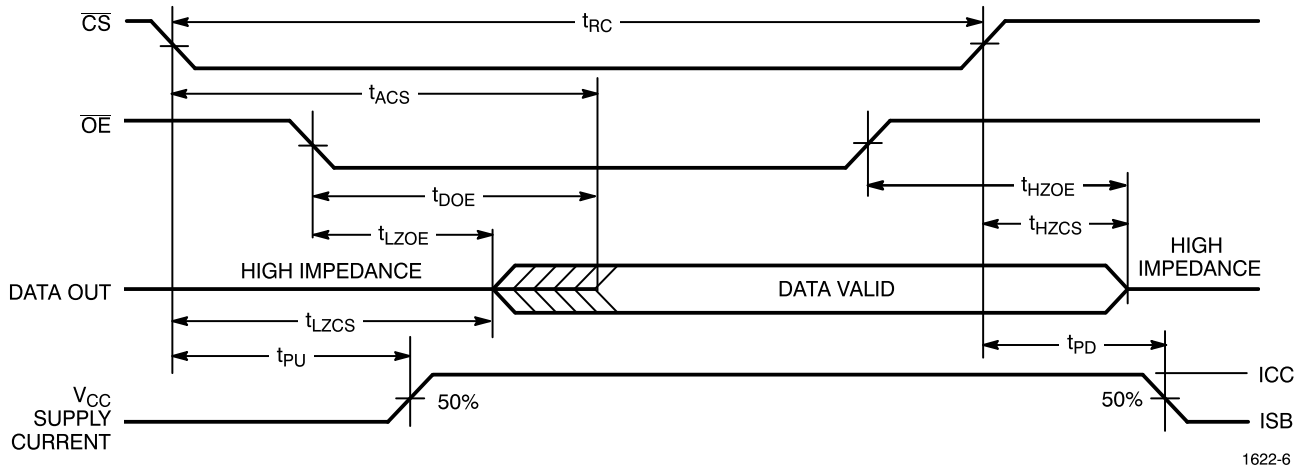
3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
5. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

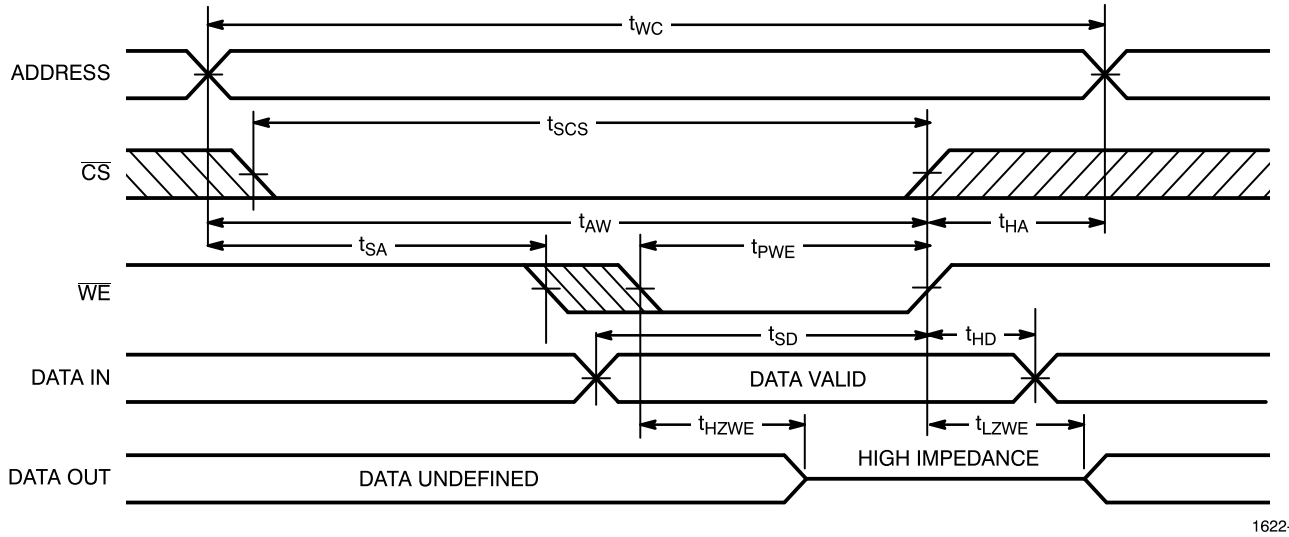
Read Cycle No. 1[6, 7]



Read Cycle No. 2[6, 8]



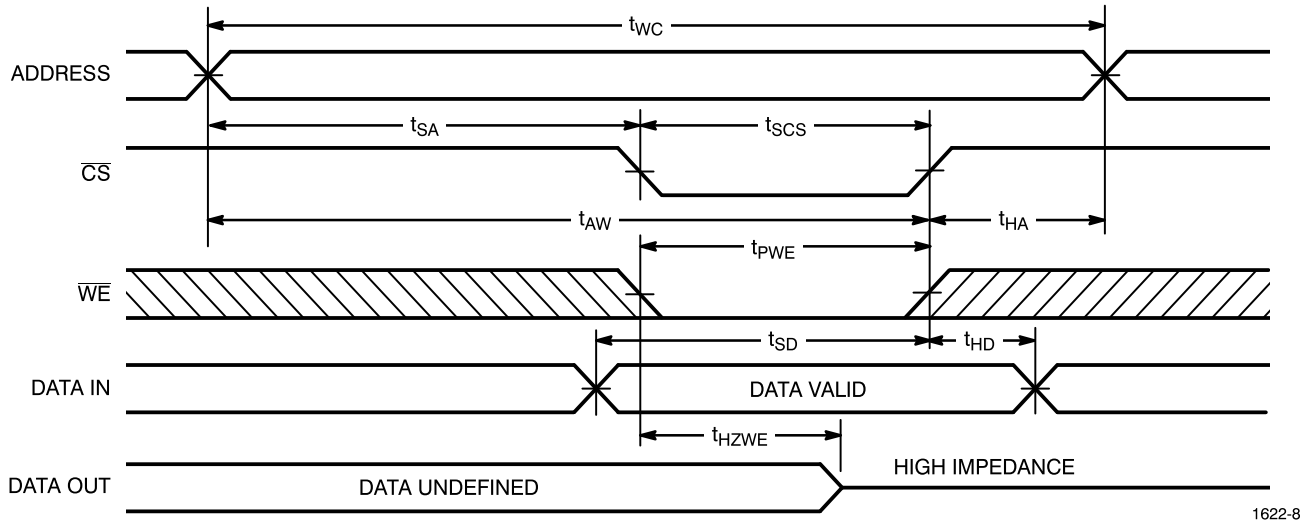
Write Cycle No. 1 ($\overline{WE}$ Controlled)[5]



Notes:
6. $\overline{WE}$ is HIGH for read cycle.
7. Device is continuously selected, $\overline{CS}$ = V_{IL}.
8. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[5, 9]



Note:
9. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Input/Output	Mode
H	X	X	High Z	Deselect/Power-Down
L	L	H	Data Out	Read
L	X	L	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
15	CYM1622PV−15C	PV04	40-Pin Plastic VDIP Module	Commercial
20	CYM1622PV−20C	PV04	40-Pin Plastic VDIP Module	Commercial
25	CYM1622PV−25C	PV04	40-Pin Plastic VDIP Module	Commercial
30	CYM1622PV−30C	PV04	40-Pin Plastic VDIP Module	Commercial
35	CYM1622PV−35C	PV04	40-Pin Plastic VDIP Module	Commercial
45	CYM1622PV−45C	PV04	40-Pin Plastic VDIP Module	Commercial

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Package Diagram

40-Pin Plastic VDIP Module PV04