CYM1720

32K x 24 Static RAM Module

Features

- **High-density 768-kilobit SRAM module**
- **High-speed CMOS SRAMs**
  — **Access time of 15 ns**
- **56-pin, 0.5-inch-high ZIP package**
- **Low active power**
  — **1.8W (max. for t_{AA} = 25 ns)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Commercial temperature range**
- **Small PCB footprint**
  — **0.66 sq. in.**

Functional Description

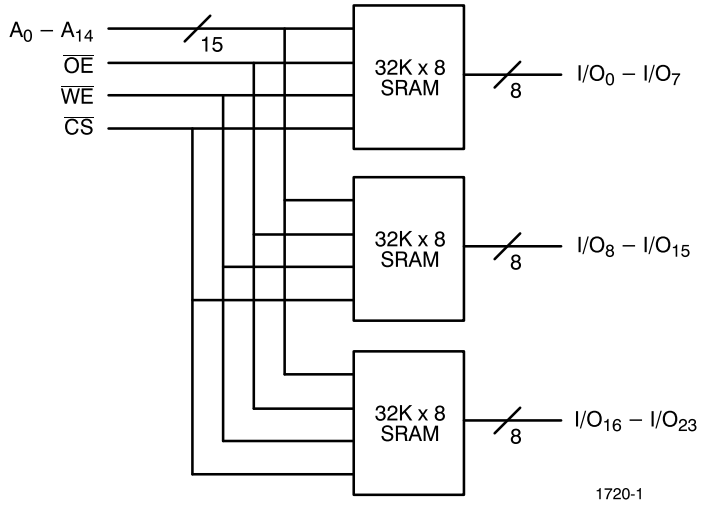
The CYM1720 is a high-performance 768-kilobit static RAM module organized as 32K words by 24 bits. This module is constructed using three 32K x 8 static RAMs in SOJ packages mounted onto an epoxy laminate board with pins.

Writing to the device is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins (I/O_0 through I/O_{23}) of the device is written into the memory location specified on the address pins (A_0 through A_{14}).

Reading the device is accomplished by taking the chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the input/output pins.

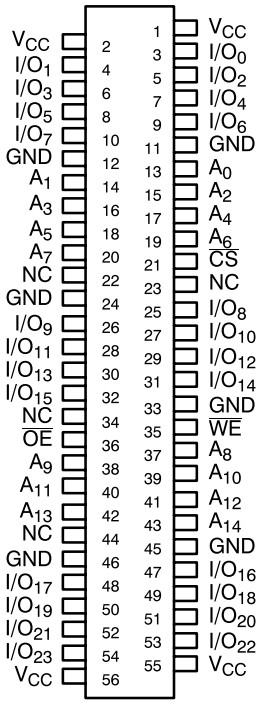
The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable is HIGH.

Logic Block Diagram



Pin Configuration

ZIP
Top View



Selection Guide

	1720–15	1720–20	1720–25	1720–30	1720–35
Maximum Access Time (ns)	15	20	25	30	35
Maximum Operating Current (mA)	450	450	330	330	330
Maximum Standby Current (mA)	120	120	60	60	60

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −55°C to +125°C

Ambient Temperature with Power Applied ..... −10°C to +85°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CYM1720−15, 20		CYM1720−25, 30, 35		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−20	+20	−20	+20	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−10	+10	−10	+10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		450		330	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		120		60	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V		90		60	mA

Shaded area contains preliminary information.

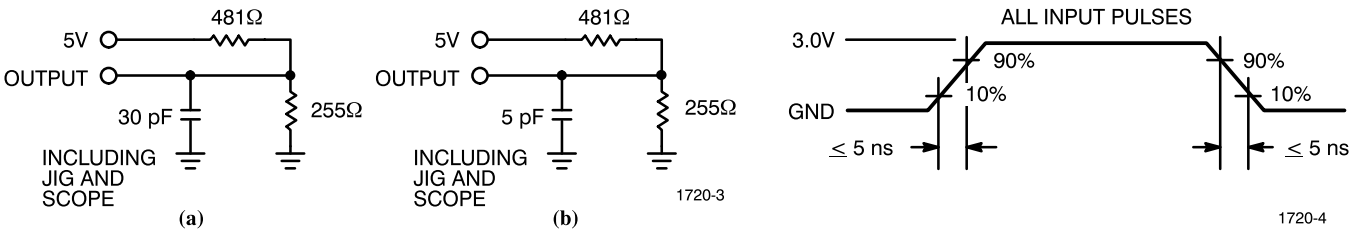
Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	35	pF
C_{OUT}	Output Capacitance		25	pF

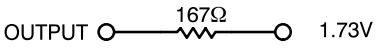
Notes:

1. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3]

Parameter	Description	1720−15		1720−20		1720−25		1720−30		1720−35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	15		20		25		30		35		ns
t_{AA}	Address to Data Valid		15		20		25		30		35	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		15		20		25		30		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		8		10		10		15		18	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		6		8		10		20		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	3		3		3		5		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		6		8		20		20		20	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		15		20		25		25		30	ns
WRITE CYCLE[6]												
t_{WC}	Write Cycle Time	15		20		25		30		35		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	10		12		20		25		30		ns
t_{AW}	Address Set-Up to Write End	10		12		20		25		30		ns
t_{HA}	Address Hold from Write End	1		2		2		5		5		ns
t_{SA}	Address Set-Up to Write Start	1		2		5		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		20		25		25		ns
t_{SD}	Data Set-Up to Write End	9		10		12		18		18		ns
t_{HD}	Data Hold from Write End	1		2		2		3		3		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5]	0	8	0	8	0	10	0	15	0	15	ns

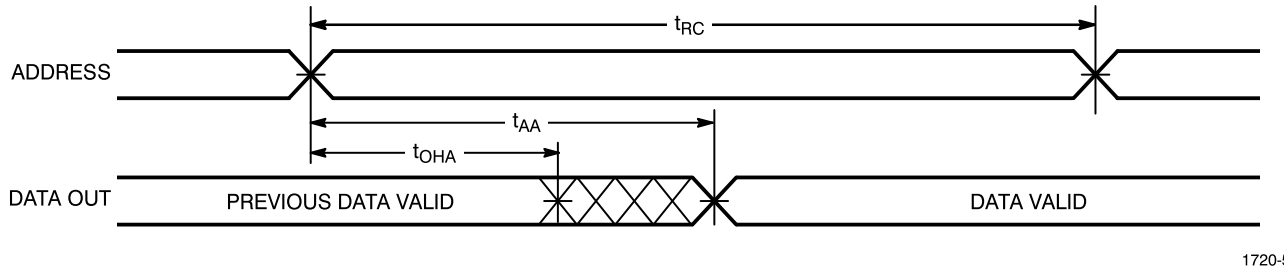
Shaded area contains preliminary information.

Notes:

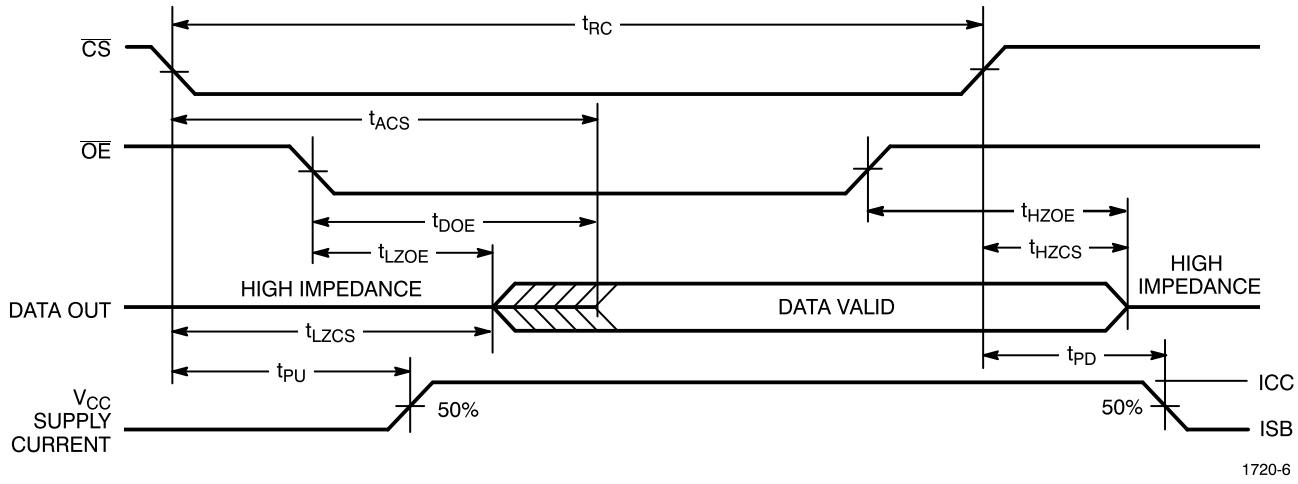
3. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device.
5. t_{HZOE}, t_{HZCS}, and t_{LZCE} are specified with C_L = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

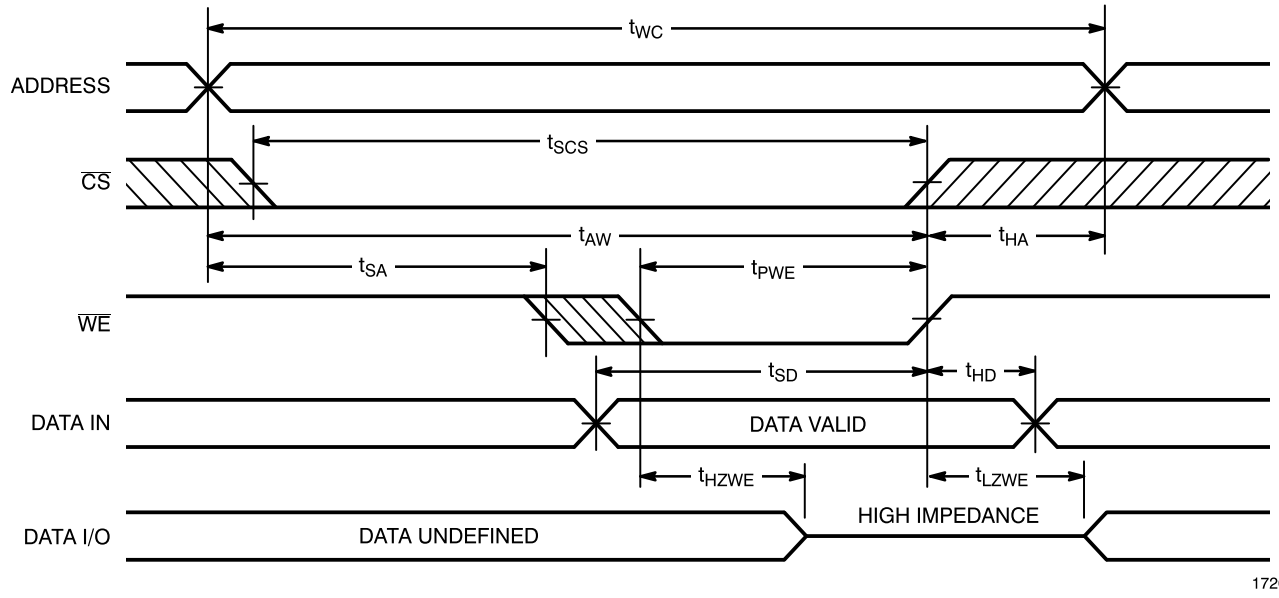
Read Cycle No. 1[7, 8]



Read Cycle No. 2[7, 9]



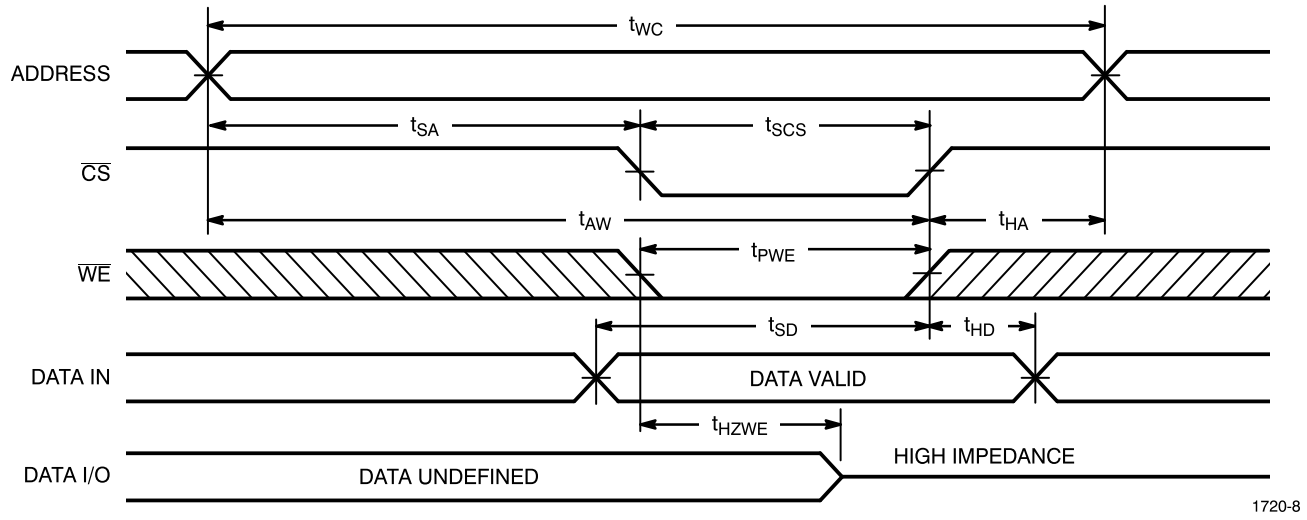
Write Cycle No. 1 ($\overline{WE}$ Controlled)[6, 10]



Notes:
7. $\overline{WE}$ is HIGH for read cycle.
8. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{OE}$= V_{IL}.
9. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
10. Data I/O will be high impedance if $\overline{OE}$ = V_{IH}.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[6, 10, 11]



Note:
11. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Input/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read Word
L	L	X	Data In	Write Word
L	H	H	High Z	Deselect

Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
15	CYM1720PZ−15C	PZ05	56-Pin ZIP Module	Commercial
20	CYM1720PZ−20C	PZ05	56-Pin ZIP Module	Commercial
25	CYM1720PZ−25C	PZ05	56-Pin ZIP Module	Commercial
30	CYM1720PZ−30C	PZ05	56-Pin ZIP Module	Commercial
35	CYM1720PZ−35C	PZ05	56-Pin ZIP Module	Commercial

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Package Diagram

56-Pin ZIP Module PZ05