PRELIMINARY **CYM1828**

32K x 32 Static RAM Module

Features

- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 25 ns**
- **66-pin, 1.1-inch-square PGA package**
- **Low active power**
  - **3.3W (max.)**
- **Hermetic SMD technology**
- **TTL-compatible inputs and outputs**
- **Commercial and military temperature ranges**

Functional Description

The CYM1828 is a very high performance 1-megabit static RAM module organized as 32K words by 32 bits. The module is constructed using four 32K x 8 static RAMs mounted onto a multilayer ceramic substrate. Four chip selects ($\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$, $\overline{CS}_4$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

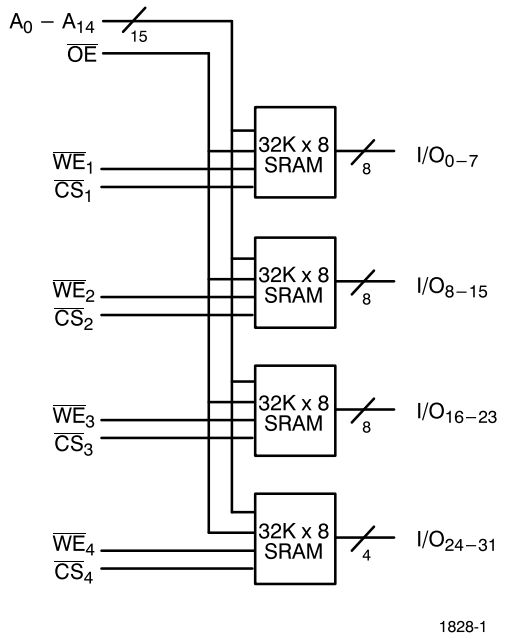
Writing to each byte is accomplished when the appropriate chip selects ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW.

Data on the input/output pins (I/O) is written into the memory location specified on the address pins (A_0 through A_{14}).

Reading the device is accomplished by taking chip selects LOW while write enable remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data input/output pins.

The data input/output pins remain in a high-impedance state when write enable is LOW or the appropriate chip selects are HIGH.

Logic Block Diagram



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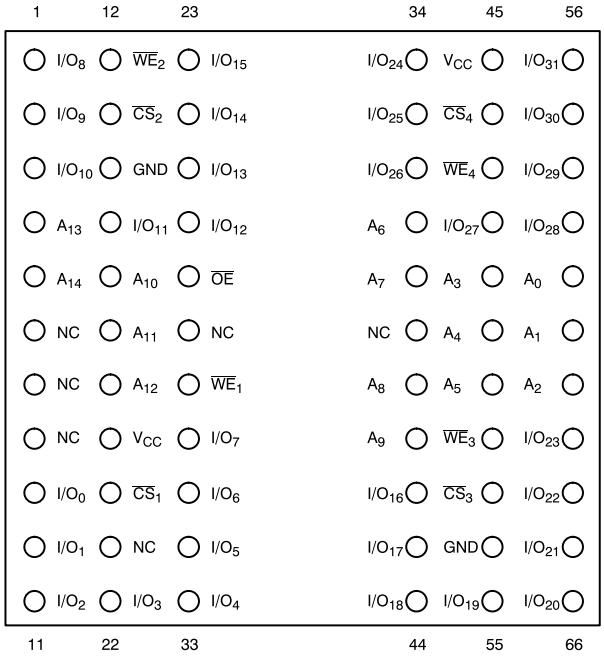
Pin Configuration

Top View



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Selection Guide

		1828–25	1828–30	1828–35	1828–45	1828–55	1828–70
Maximum Access Time (ns)		25	30	35	45	55	70
Maximum Operating Current (mA)	Commercial	600	600	600	600	600	600
	Military			600	600	600	600
Maximum Standby Current (mA)	Commercial	200	200	200	200	200	200
	Military			200	200	200	200

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature ..... −65°C to +150°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		1828 Min.	1828 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}+0.3	V
V_{IL}	Input LOW Voltage			−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}, V_{CC} = Max.		−20	+20	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−20	+20	µA
I_{CCx32}	V_{CC} Operating Supply Current by 32 Mode	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}			600	mA
			L Version		400	
I_{CCx16}	V_{CC} Operating Supply Current by 16 Mode	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}			360	mA
			L Version		230	
I_{CCx8}	V_{CC} Operating Supply Current by 8 Mode	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}			240	mA
			L Version		145	
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}; $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%			200	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}; $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V			100	mA

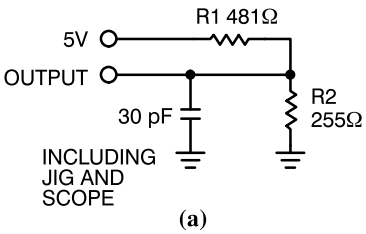
Capacitance[2]

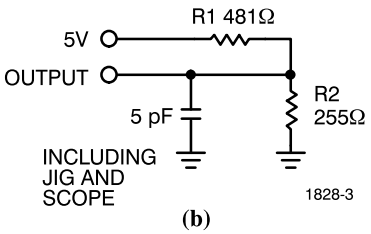
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	50	pF
C_{OUT}	Output Capacitance		20	pF

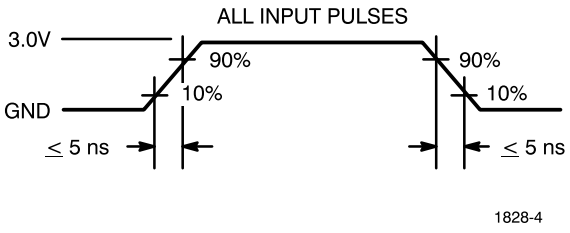
Notes:

1. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.

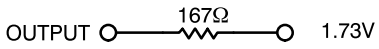
AC Test Loads and Waveforms







Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3]

Parameter	Description	1828−25		1828−30		1828−35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		30		35		ns
t_{AA}	Address to Data Valid		25		30		35	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		30		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		17		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		15		15		25	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	3		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		15		15		25	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	25		30		35		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		25		30		ns
t_{AW}	Address Set-Up to Write End	20		25		30		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		25		ns
t_{SD}	Data Set-Up to Write End	15		20		17		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5]	0	15	0	20	0	30	ns

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed by design and not 100% tested.
5. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics Over the Operating Range (continued)[3]

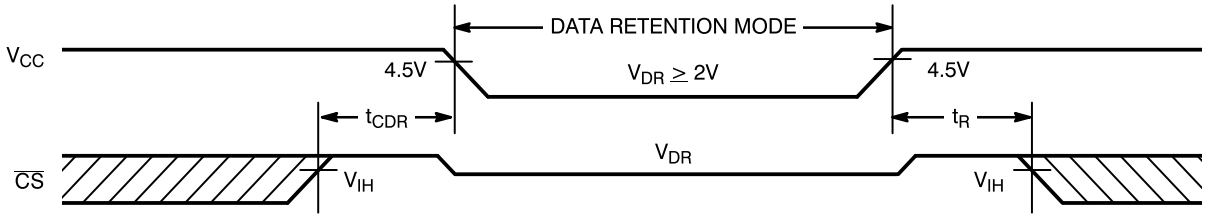
Parameter	Description	1828−45		1828−55		1828−70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	45		55		70		ns
t_{AA}	Address to Data Valid		45		55		70	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		45		55		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		30		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		25		30		30	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	3		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		25		30		30	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	45		55		70		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	40		45		55		ns
t_{AW}	Address Set-Up to Write End	40		45		55		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	30		35		45		ns
t_{SD}	Data Set-Up to Write End	25		30		40		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5]	0	30	0	30	0	30	ns

Data Retention Characteristics (L Version Only)

Parameter	Description	Test Conditions	1828		Unit
			Min.	Max.	
V_{DR}	V_{CC} for Retention Data	$\overline{CS} \geq V_{CC} - 0.2V$	2		V
I_{CCDR3}	Data Retention Current	$\overline{CS} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $V_{DR} = 3.0V$		320	µA
t_{CDR}[7]	Chip Deselect to Data Retention Time		0		ns
t_R[7]	Operation Recovery Time		t_{RC}		ns

Note:
7. Guaranteed, not tested.

Data Retention Waveform



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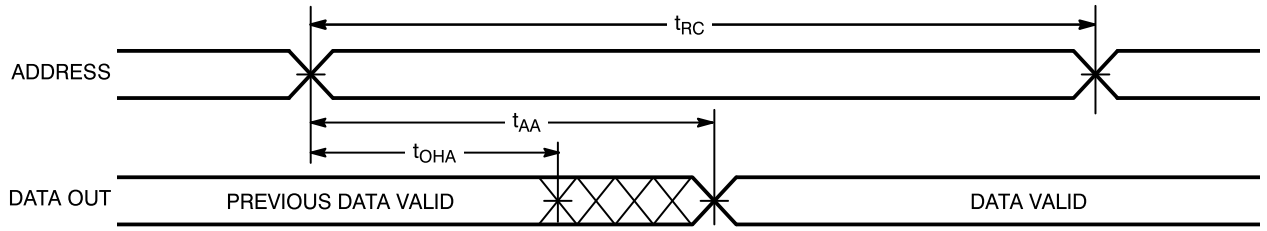
Switching Waveforms

Read Cycle No. 1[8, 9]



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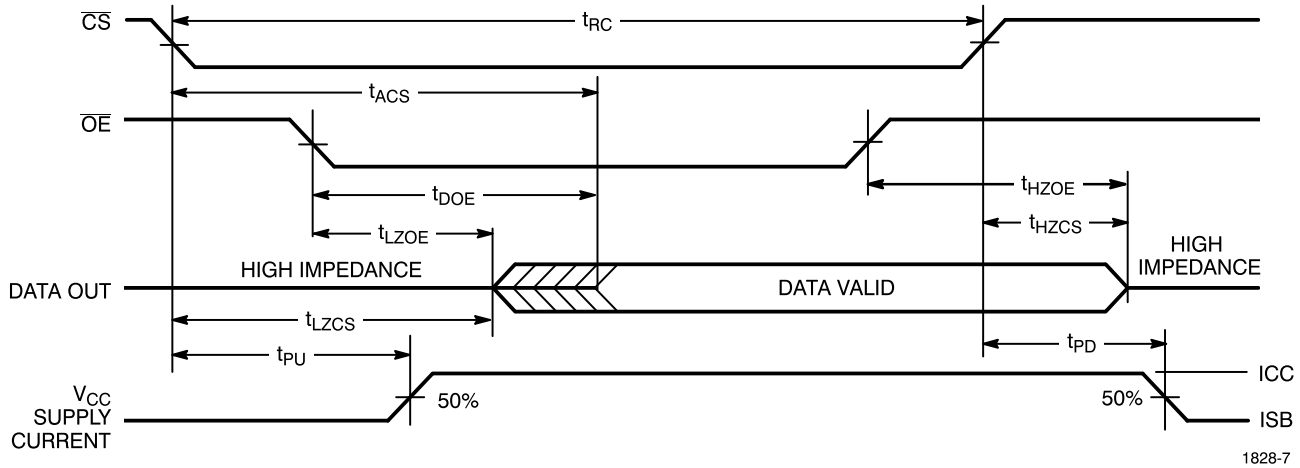
Read Cycle No. 2[8, 10]



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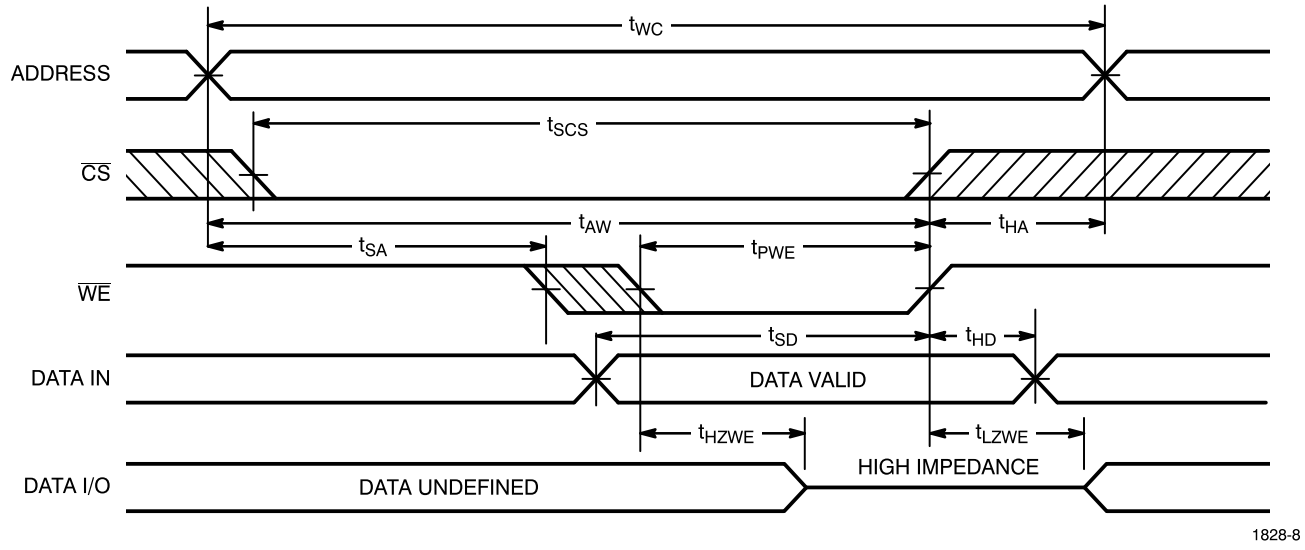
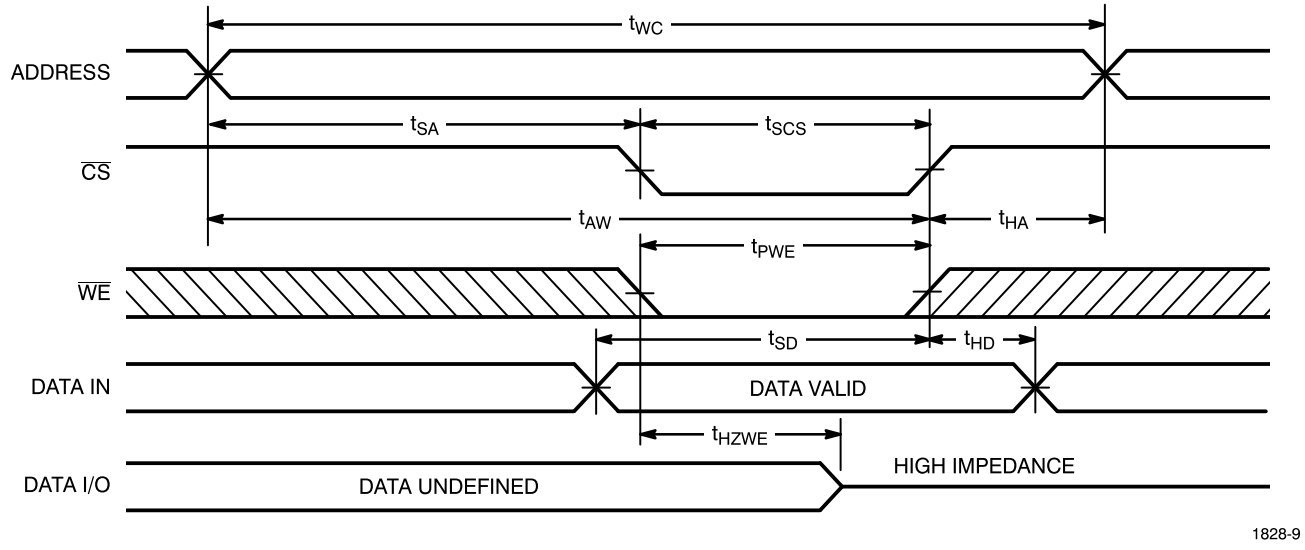
Notes:
8. $\overline{WE}_N$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{OE}$= V_{IL}.
10. Address valid prior to or coincident with $\overline{CS}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{WE}$ Controlled)[6, 11]



Write Cycle No. 2 ($\overline{CS}$ Controlled)[6, 11, 12]



Notes:
11. Data I/O will be high impedance if $\overline{OE}$ = V_{IH}.
12. If $\overline{CS}_N$ goes HIGH simultaneously with $\overline{WE}_N$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}_N$	$\overline{OE}$	$\overline{WE}_N$	Input/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	L	H	Data Out	Read
L	X	L	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CYM1828HG−25C	HG01	66-Pin PGA Module	Commercial
30	CYM1828HG−30C	HG01	66-Pin PGA Module	Commercial
35	CYM1828HG−35C	HG01	66-Pin PGA Module	Commercial
	CYM1828LHG−35C	HG01	66-Pin PGA Module	
	CYM1828HG−35MB	HG01	66-Pin PGA Module	Military
	CYM1828LHG−35MB	HG01	66-Pin PGA Module	
45	CYM1828HG−45C	HG01	66-Pin PGA Module	Commercial
	CYM1828LHG−45C	HG01	66-Pin PGA Module	
	CYM1828HG−45MB	HG01	66-Pin PGA Module	Military
	CYM1828LHG−45MB	HG01	66-Pin PGA Module	
55	CYM1828HG−55C	HG01	66-Pin PGA Module	Commercial
	CYM1828LHG−55C	HG01	66-Pin PGA Module	
	CYM1828HG−55MB	HG01	66-Pin PGA Module	Military
	CYM1828LHG−55MB	HG01	66-Pin PGA Module	
70	CYM1828HG−70C	HG01	66-Pin PGA Module	Commercial
	CYM1828LHG−70C	HG01	66-Pin PGA Module	
	CYM1828HG−70MB	HG01	66-Pin PGA Module	Military
	CYM1828LHG−70MB	HG01	66-Pin PGA Module	

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Package Diagram

66-Pin PGA Module HG01