CYM1840

256K x 32 Static RAM Module

Features

- **High-density 8-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 20 ns**
- **Independent byte and word controls**
- **Low active power**
  - **6.2W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of .350 in.**
- **Small PCB footprint**
  - **1.8 sq. in.**

Functional Description

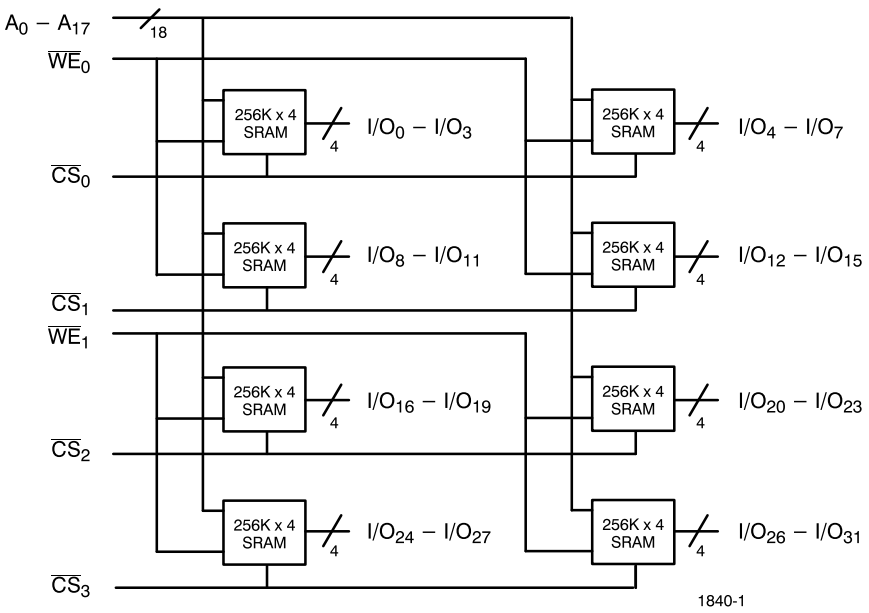
The CYM1840 is a high-performance 8-megabit static RAM module organized as 256K words by 32 bits. This module is constructed from eight 256K x 4 SRAMs in SOJ packages mounted on an epoxy laminate substrate with pins. Four chip selects ($\overline{CS}_0$, $\overline{CS}_1$, $\overline{CS}_2$, and $\overline{CS}_3$) are used to independently enable the four bytes. Two write enables ($\overline{WE}_0$ and $\overline{WE}_1$) are used to independently write to either the upper or lower 16-bit word of RAM. Reading or writing can be executed on individual bytes or on any combination of multiple bytes through the proper use of selects and write enables.

Writing to each byte is accomplished when the appropriate chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins ($\overline{I/O}_X$) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking the chip selects ($\overline{CS}$) LOW, while write enables ($\overline{WE}$) remain HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data input/output pins ($\overline{I/O}$).

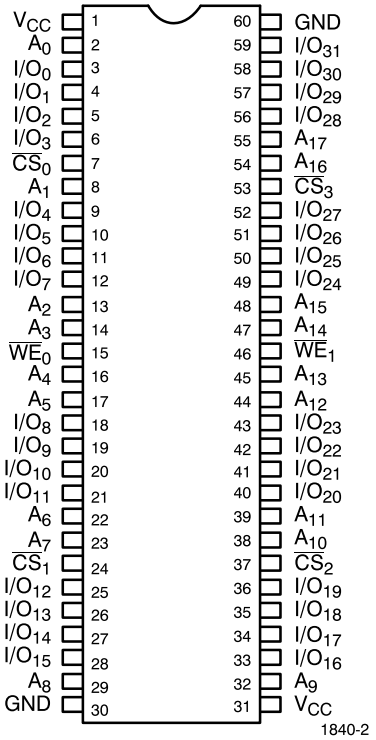
The data input/output pins stay in the high-impedance state when write enables ($\overline{WE}$) are LOW or the appropriate chip selects are HIGH.

Logic Block Diagram



Pin Configuration

DIP
Top View



Selection Guide

	1840–20	1840–25	1840–30	1840–35	1840–45	1840–55
Maximum Access Time (ns)	20	25	30	35	45	55
Maximum Operating Current (mA)	1120	1120	1120	1120	1120	1120
Maximum Standby Current (mA)	320	320	320	320	320	320

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied (PD) ..... −10°C to +85°C

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CYM1840		Unit
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−20	+20	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−50	+50	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}_X$ ≤ V_{IL}		1120	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}_X$ ≥ V_{IH}, Min. Duty Cycle = 100%		320	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}_X$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V		160	mA

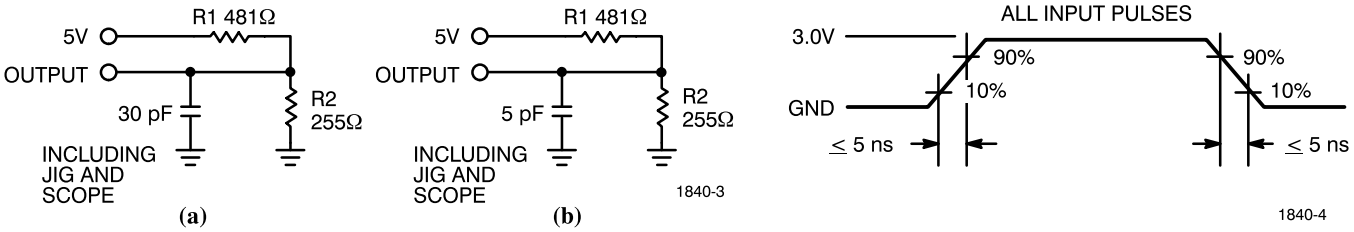
Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{INA}	Input Capacitance, Address Pins	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	100	pF
C_{INB}	Input Capacitance, I/O Pins		30	pF
C_{OUT}	Output Capacitance		30	pF

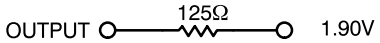
Notes:

1. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[3]

Parameter	Description	1840−20		1840−25		1840−30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	20		25		30		ns
t_{AA}	Address to Data Valid		20		25		30	ns
t_{OHA}	Output Hold from Address Change	5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		20		25		30	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	5		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		20		20		20	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		20		25		30	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	20		25		30		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	18		20		25		ns
t_{AW}	Address Set-Up to Write End	18		20		25		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		20		25		ns
t_{SD}	Data Set-Up to Write End	13		15		15		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5]	0	15	0	15	0	15	ns

Notes:

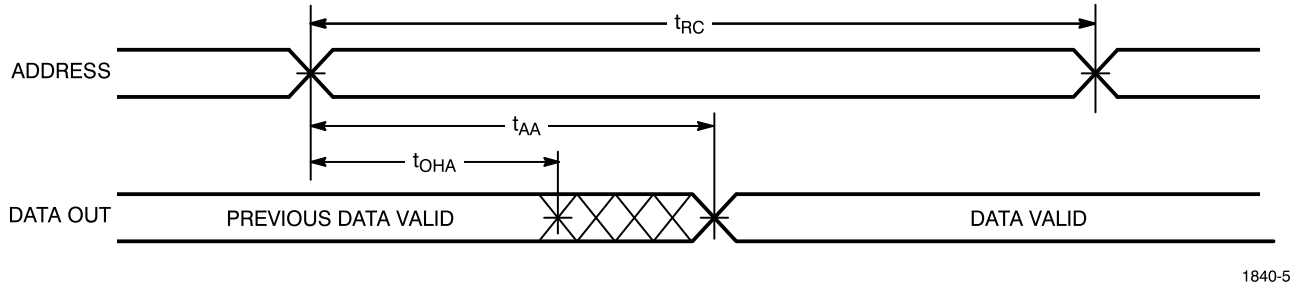
3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device.
5. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady-state voltage.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Characteristics Over the Operating Range[3] (continued)

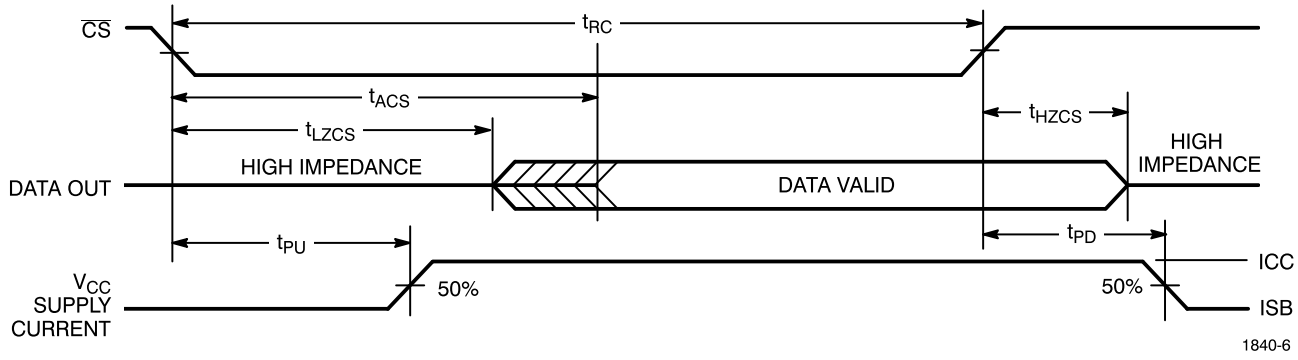
Parameter	Description	1840−35		1840−45		1840−55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid		35		45		55	ns
t_{OHA}	Output Hold from Address Change	5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		35		45		55	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[4]	5		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		25		25		25	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		35		45		55	ns
WRITE CYCLE[6]								
t_{WC}	Write Cycle Time	35		45		55		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	30		40		50		ns
t_{AW}	Address Set-Up to Write End	30		40		50		ns
t_{HA}	Address Hold from Write End	6		6		6		ns
t_{SA}	Address Set-Up to Write Start	6		6		6		ns
t_{PWE}	$\overline{WE}$ Pulse Width	25		30		40		ns
t_{SD}	Data Set-Up to Write End	25		30		35		ns
t_{HD}	Data Hold from Write End	6		6		6		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5]	0	25	0	25	0	25	ns

Switching Waveforms

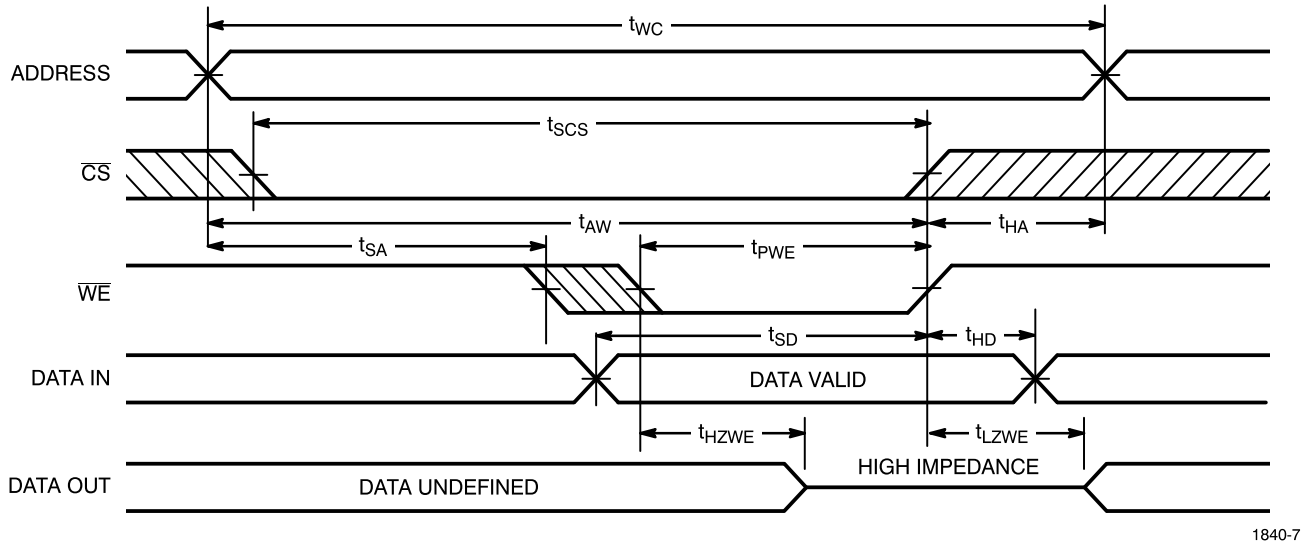
Read Cycle No. 1[7, 8]



Read Cycle No. 2[7, 8]



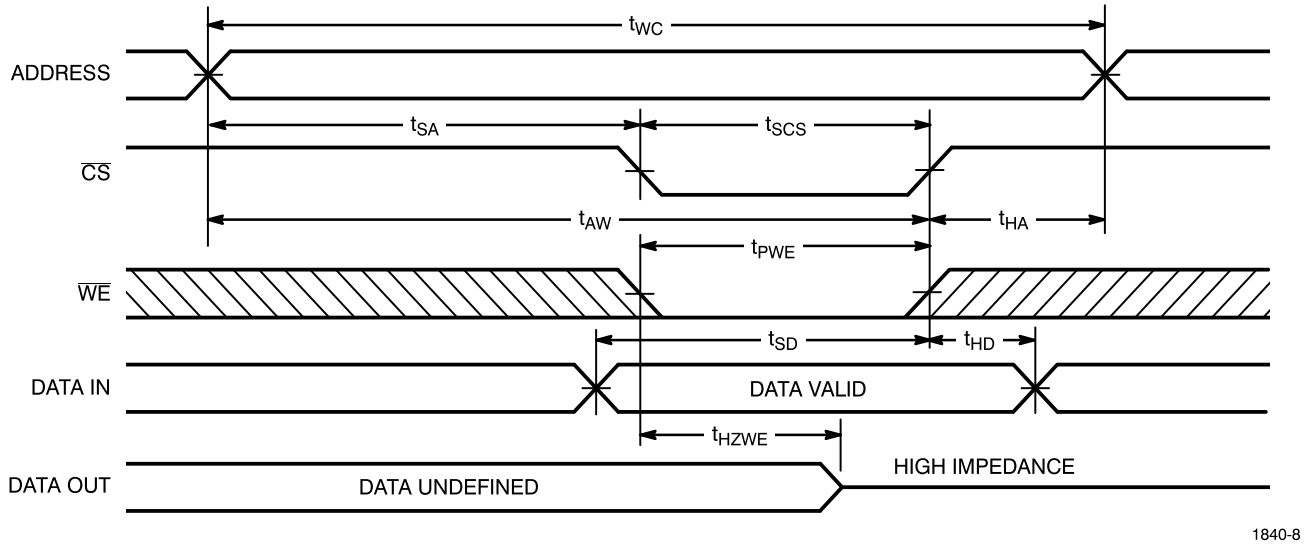
Write Cycle No. 1 ($\overline{WE}$ Controlled)[6]



Notes:
7. Device is continuously selected, $\overline{CS} = V_{IL}$.
8. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[6, 9]



Note:
9. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Truth Table

$\overline{CS}$	$\overline{WE}$	Input/Output	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

Ordering Information

Speed	Ordering Code	Package Name	Package Type	Operating Range
20	CYM1840PD−20C	PD06	60-Pin DIP Module	Commercial
25	CYM1840PD−25C	PD06	60-Pin DIP Module	Commercial
30	CYM1840PD−30C	PD06	60-Pin DIP Module	Commercial
35	CYM1840PD−35C	PD06	60-Pin DIP Module	Commercial
45	CYM1840PD−45C	PD06	60-Pin DIP Module	Commercial
55	CYM1840PD−55C	PD06	60-Pin DIP Module	Commercial

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Package Diagram

60-Pin DIP Module PD06