CYM7232
CYM7264

DRAM Accelerator Module

Features

- **4-megabyte to 1-gigabyte control capability**
- **32- or 64-bit bus interface (M7232 only)**
- **32- or 64-bit EDC versions**
  — **1-bit correct; 2-bit detect**
- **Multiplexed or non-multiplexed bus**
- **i486, Pentium™, i860, 68040, 88110, PowerPC™, SPARC, and MIPS compatible**
- **Synchronous bus interface**
- **25-, 33-, and 40-MHz versions**
- **Error-logging facilities**
- **Cache line fill burst support; posted writes**
- **Cache line write-back support; write FIFO**
- **High performance**
  — **25-ns writes**
  — **175-, 25-, 50-, 25-ns burst read/80-ns DRAMs**
- **Automatic refresh with scrubbing**
- **Multiprocessor compatible**
  — **Inhibited reads and writes**
  — **Reflective reads**
  — **Reads for ownership**
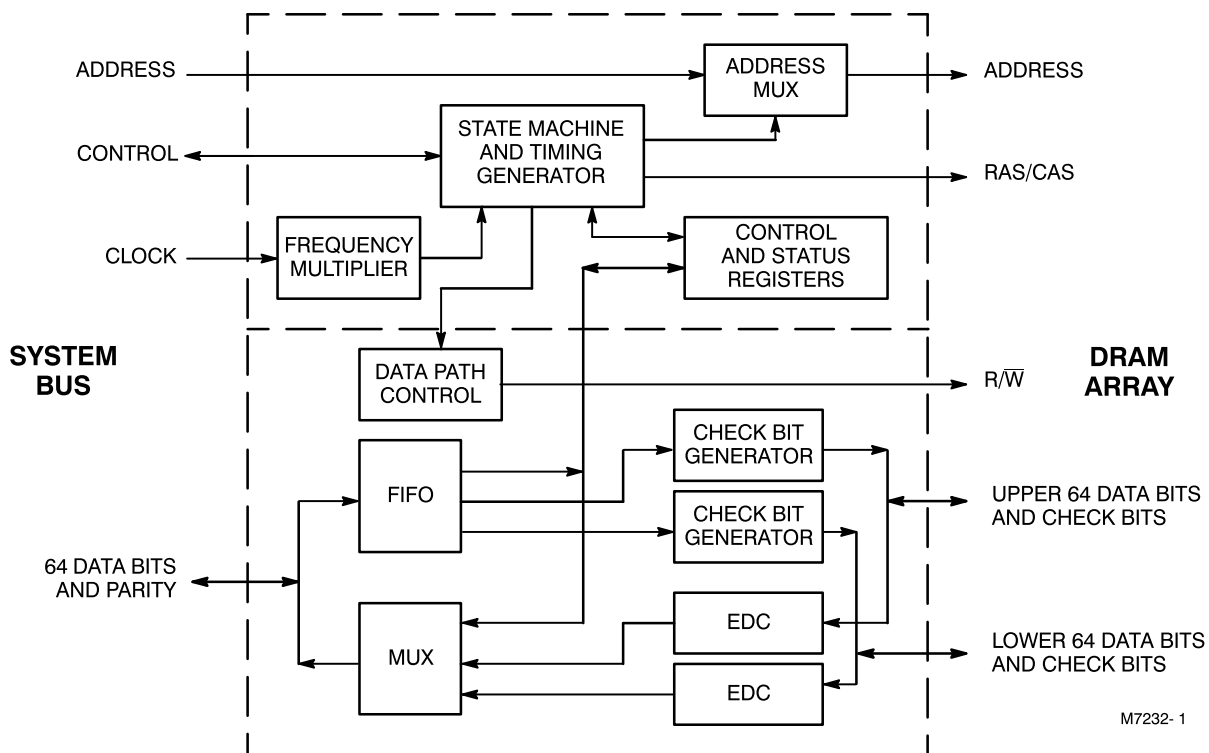- **Bus parity generation and checking**
- **Very small size**

Functional Description

The CYM7232 and the CYM7264 consist of a full-function DRAM controller and a pipelined/FIFO data multiplexer/demultiplexer with error correction for cache-based, uniprocessor, and multiprocessor systems memory control. The CYM7232 performs 32-bit Error Detection and Correction (EDC) while CYM7264 performs 64-bit EDC. They both connect to the system bus through a 64-bit-wide data bus, and a 36-bit wide address bus. The CYM7232 also supports 32-bit system buses. The bus transfer control signals support i486, Pentium, i860, 68040, 88110, SPARC MBus, MIPS R4000, or other interfaces. The controller module interfaces to the DRAM array through a 16-byte-wide data bus plus check bits, a 12-bit row/column address bus, four $\overline{RAS}$ outputs, four $\overline{CAS}$ outputs, and four read/write control lines.

During write operations, data passes from the system bus through a FIFO array that acts as an incoming queue. Writes occur at the system bus speed until the FIFO is full (sixteen 64-bit words). The FIFO supports cache-line copy-back and fill operations, reducing system bus traffic to a minimum. The module supports posted writes, by suspending the actual write to DRAM until the cache-line read is completed during cache-line write-back. This speeds cache-line fill operations. The module pipelines a 16-byte-wide DRAM access into the data path for EDC, and multiplexes the data to the system bus during reads. This supports high-speed burst line fills with error corrected data. Reads and writes may be inhibited for multiprocessor support. Inhibited reads may be turned into reflective reads, and inhibited writes may be turned into reads-for-ownership.

Logic Block Diagram

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