PRELIMINARY

CYM7420
CYM7421

82420 PCIset-Compatible Level II Cache Modules

Features

- **128 Kbytes (CYM7420), 256 Kbytes (CYM7421) cache module organized as 32K by 32 or 64K by 32**
- **Tag width of 7/8 bits plus valid bit**
- **Independent dirty bit**
- **Operates with systems based on the Intel™ 82420 core logic**
- **Zero-wait state operation at 33 Mhz**
- **Constructed using standard asynchronous SRAMs**
- **112-pin Burndy Connector, Part Number CELP2X56SC3Z48**
- **Single 5V (±5%) power supply**
- **TTL-compatible inputs/outputs**

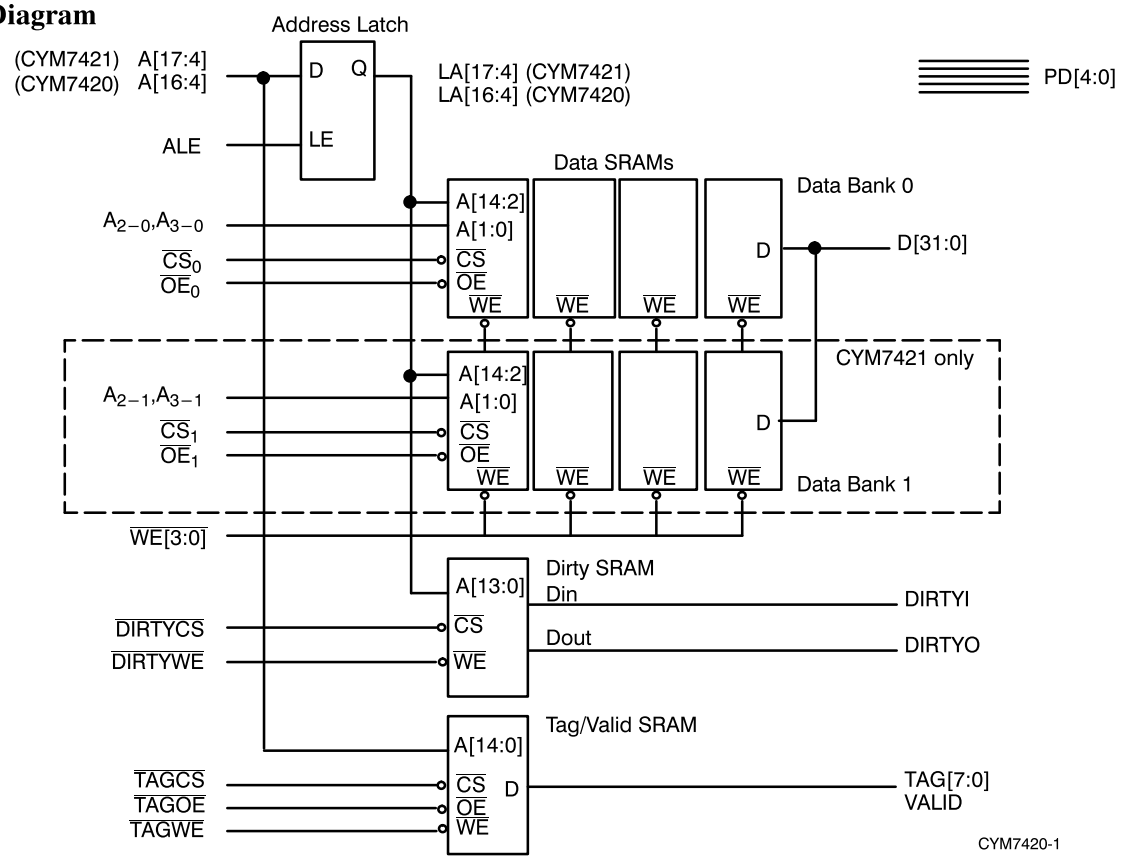
Functional Description

The CYM7420 module series is a family of cache memory subsystems for Intel 486-based systems. Each module contains either one or two banks of 32-bit wide Data SRAM, 8K/32K entries of 7/8-bit tag, and one Valid bit, and a single bit wide, separate I/O Dirty SRAM. CYM7420 has 8-bit tags, while CYM7421 support 7-bit tags. The address signals for the Data and Dirty SRAMs are latched.

The modules are configured as a 112-pin card-edge memory module. It is constructed using standard asynchronous SRAMs in SOJ packages mounted on a multilayer epoxy laminate (FR4) substrate. The module dimensions are 3.145 inches long by 1.105 inches high by 0.365 inches thick.

These modules are designed for zero wait state operation in 486-based systems operating at a bus speed of 33 Mhz. They are designed for compatibility with the Intel 82420 PCIset and other chip sets. The baseline speed grade is built using 12 nanosecond Tag SRAMs and 20 nanosecond Data SRAMs.

Logic Block Diagram



Selection Guide

	CYM7420PB–20	CYM7421PB–20
Cache Size (KB)	128	256
Data SRAM (ns)	20	20
Dirty SRAM (ns)	15	15
Tag/Valid SRAM (ns)	12	12

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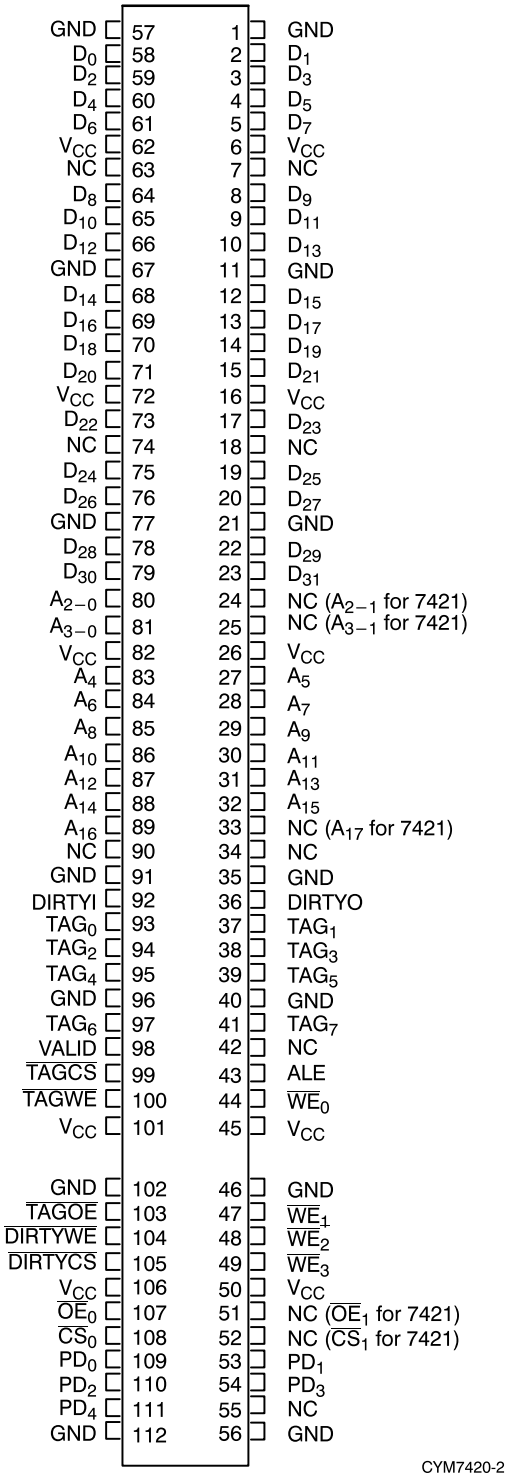
Pin Configuration

Dual Read-out SIMM
Top View



CYM7420-2

Pin Descriptions

Name	Description
A[18:4]	Host Address Bus
A_3-A_0	Host Address Bit 3, Bank 0
A_2-A_0	Host Address Bit 2, Bank 0
D[31:0]	Host Data Bus
$\overline{CS}_0$	Bank 0 Chip Set
$\overline{WE}$[3:0]	Cache Byte Write Enables
$\overline{OE}_0$	Bank 0 Output Enable
ALE	Address Latch Enable
TAG[7:0]	Tag Data Bus
VALID	Valid Bit
$\overline{TAGCS}$	Tag Chip Select
$\overline{TAGOE}$	Tag Output Enable
$\overline{TAGWE}$	Tag Write Enable
DIRTYI	Dirty Bit Input
DIRTYO	Dirty Bit Output
$\overline{DIRTYCS}$	Dirty Chip Select
$\overline{DIRTYWE}$	Dirty Write Enable
PD[4:0]	Presence Detect Output Pins
NC	No Connection
A_3-A_1	Host Address Bit 3, Bank 1
A_2-A_1	Host Address Bit 2, Bank 1
$\overline{CS}_1$	Bank 1 Chip Select
$\overline{OE}_1$	Bank 1 Output Enable

Presence Detect Table

	PD_4	PD_3	PD_2	PD_1	PD_0
CYM7420	V_{CC}	NC	NC	NC	V_{CC}
CYM7421	V_{CC}	NC	NC	V_{CC}	NC

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... 0°C to +70°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CYM7420 CYM7421 Min.	CYM7420 CYM7421 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}+0.3	V
V_{IL}	Input LOW Voltage		−0.5	0.8	V
I_{CC}	V_{CC} Operating Supply Current (CYM7420 only).	V_{CC}=MAX, I_{OUT}=0 mA, f=f_{MAX}		1050	mA
I_{CC}	V_{CC} Operating Supply Current (CYM7421 only).	V_{CC}=MAX, I_{OUT}=0 mA, f=f_{MAX}		1800	mA

Ordering Information

Cache Size	Ordering Code	Package Name	Package Type	Operating Range
128 Kbyte	CYM7420PB−20C	PM09	112-Pin Dual-Readout SIMM	Commercial
256 Kbyte	CYM7421PB−20C	PM10	112-Pin Dual-Readout SIMM	

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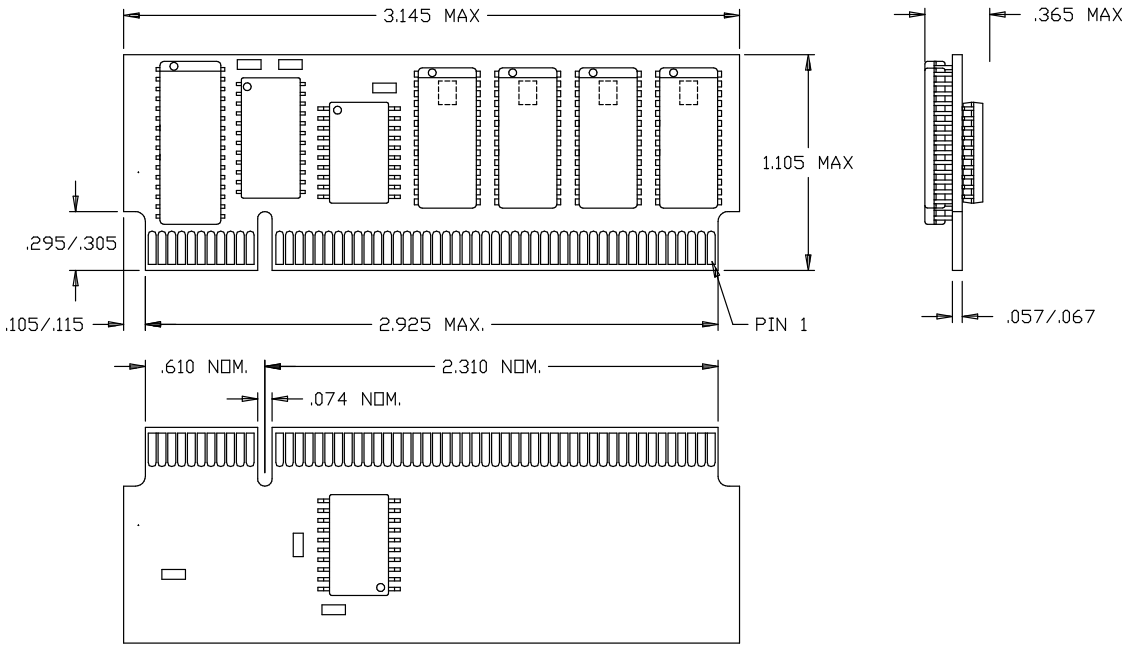
Package Diagrams

112-Pin Dual-Readout SIMM PM09



112-Pin Dual-Readout SIMM PM10