CYM7424
CYM7425

128K/256K Cache Module for the Intel™ 82420EX PCIset

Features

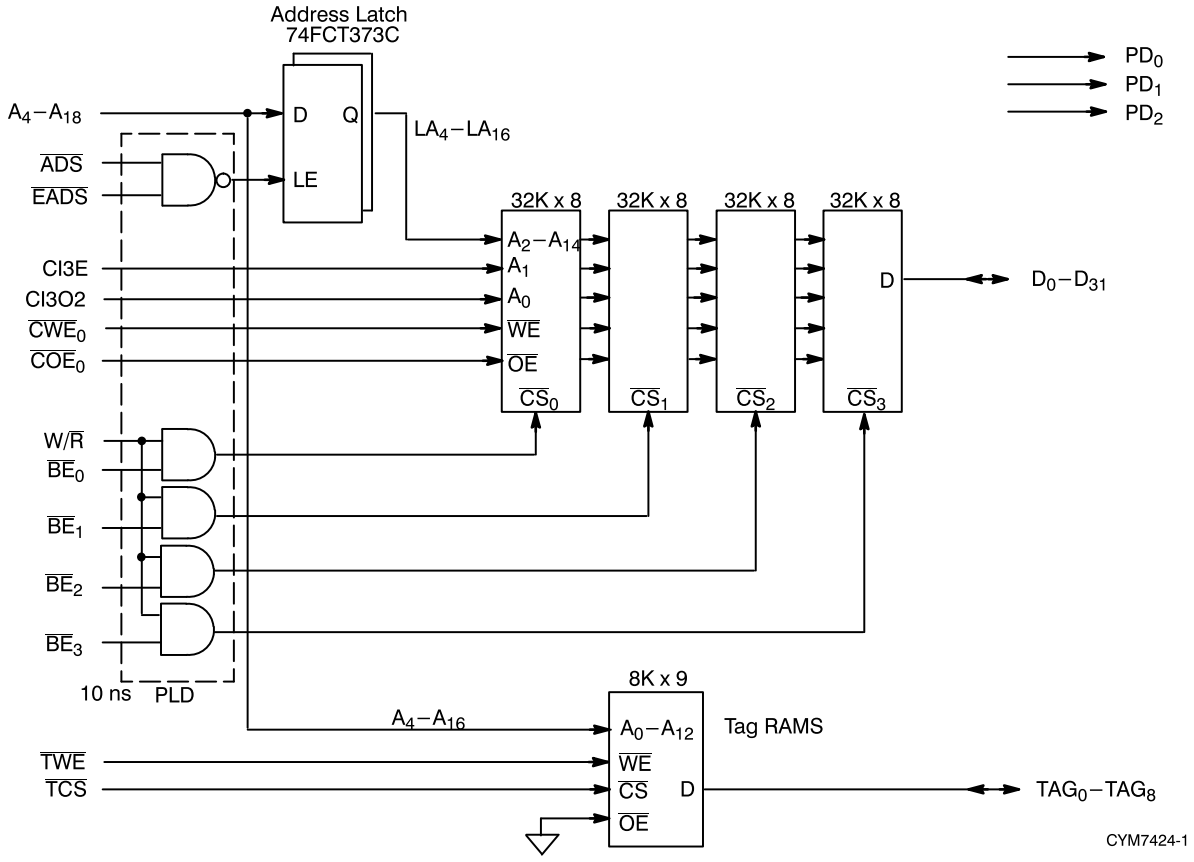
- **128 Kbyte (CYM7424) or 256 Kbyte (CYM7425) secondary cache module organized as 32K by 32 or 64K by 32**
- **Ideal for Intel 486-based systems with the 82420EX PCIset**
- **Supports 486 CPUs running at clock speeds up to 50 MHz**
- **Constructed using cost-effective CMOS asynchronous SRAMs**
- **On-board decoupling capacitors offer improved noise immunity**
- **112-position Burndy connector, part # CELP2X56SC3Z48**
- **5V (±5%) power supply**
- **TTL-compatible inputs/outputs**

Functional Description

These modules are designed specially to function as the secondary cache in Intel 486-based systems with the 82420EX (Aries) PCIset. Each module contains either one or two banks of 32-bit wide data SRAMs, a 9-bit wide tag, address latch, and byte write logic. Asynchronous CMOS SRAMs are used to provide a high-performance, low-cost, and low-power solution for CPU speeds up to 50 MHz. Multiple ground pins and on-board decoupling capacitors ensure maximum protection from noise.

Each module interfaces with the rest of the system via a 112-pin Burndy connector. All components on the cache module are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. The package dimensions are 3.145″ x 0.380″ x 1.105″. All inputs and outputs of the CYM7424 and CYM7425 cache modules are TTL compatible and operate from a single 5V power supply. The contact pins are plated with 100 micro-inches of nickel covered by 10 micro-inches of gold flash.

Logic Block Diagram CYM7424



Selection Guide

	CYM7424–20	CYM7425–20
Cache Size (KB)	128	256
Data SRAM (ns)	20	20
Tag/Valid SRAM (ns)	15	15

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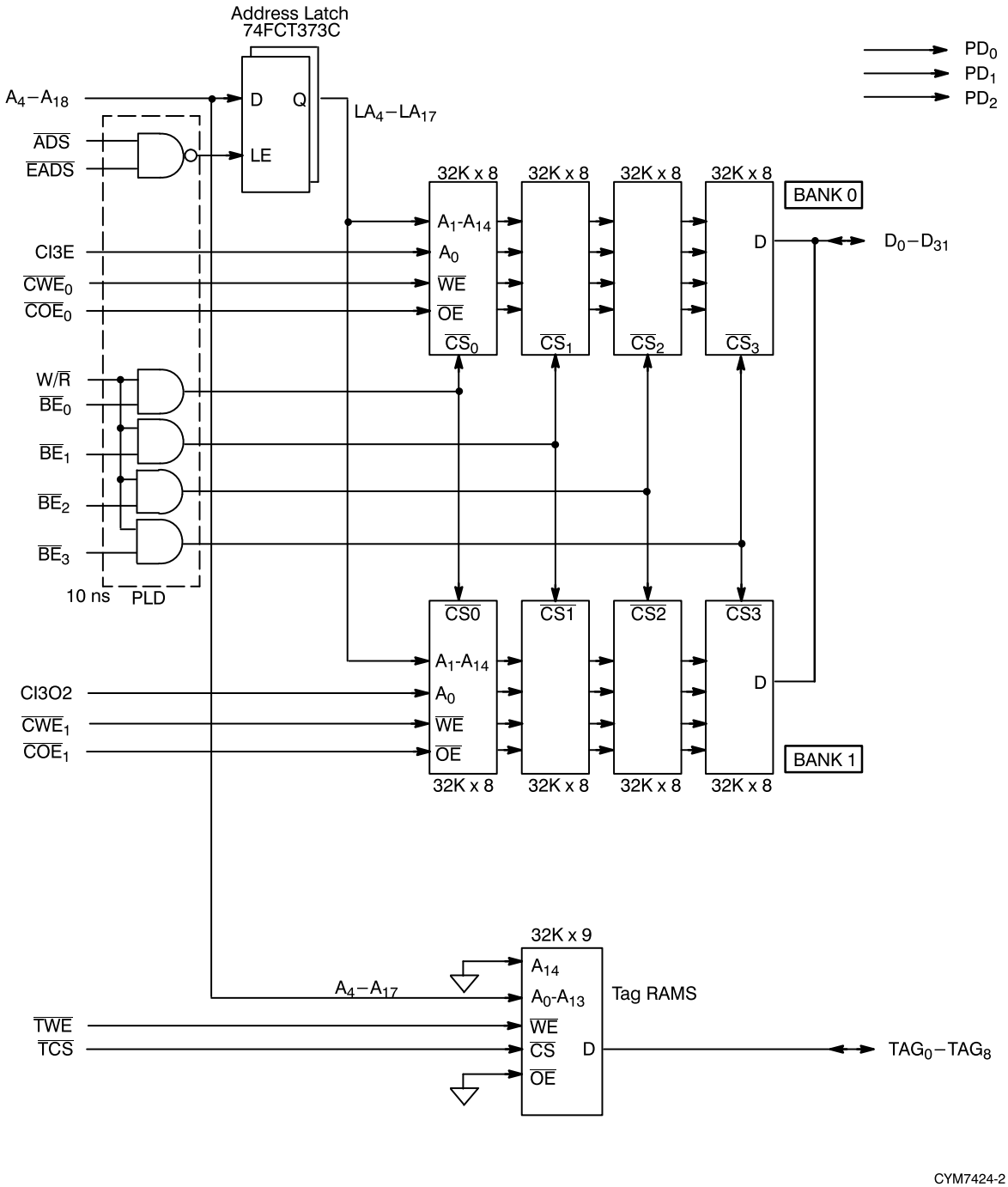
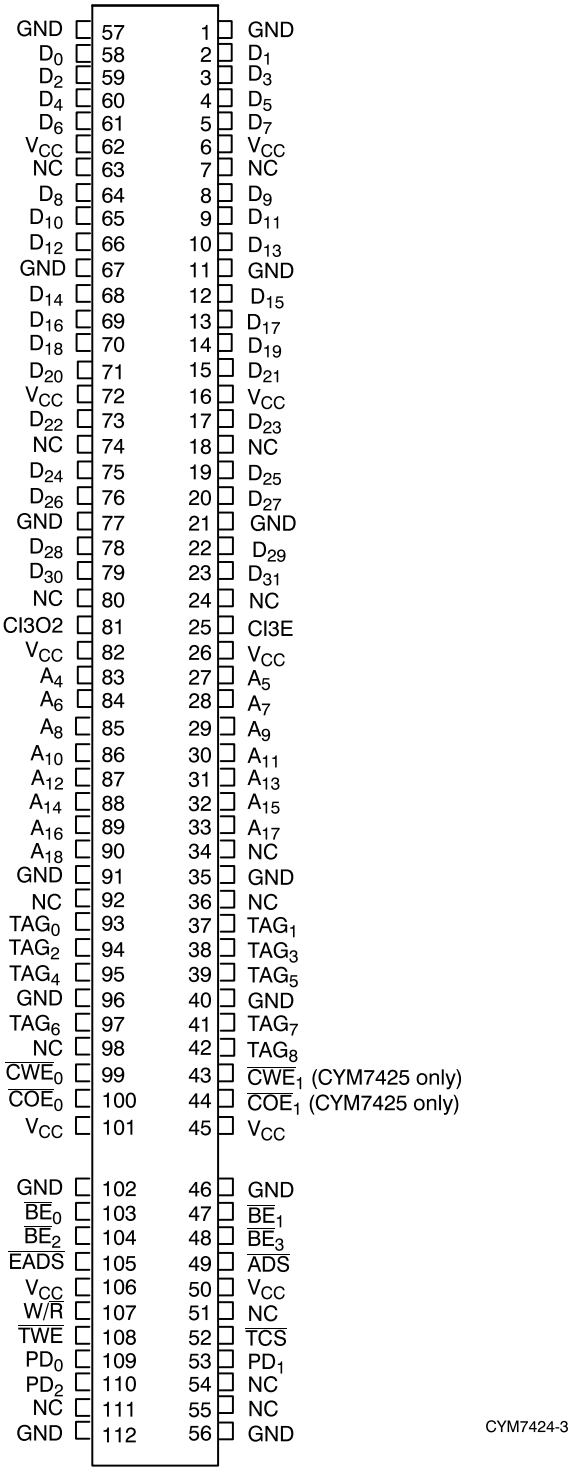
Logic Block Diagram CYM7425



Pin Configuration

Dual Read-out SIMM
Top View



CYM7424-3

Pin Descriptions

Name	Description
A_4-A_{18}	Cache Address Inputs
CI3O2, CI3E	Cache Index Address Inputs
D_0-D_{31}	Cache Data Input/Outputs
$\overline{BE}_0-\overline{BE}_3$	Byte Enable Inputs
$\overline{CWE}_0$	Bank 0 Write Enable Input
$\overline{CWE}_1$	Bank 1 Write Enable Input
$\overline{COE}_0$	Bank 0 Output Enable
$\overline{COE}_1$	Bank 1 Output Enable
$W/\overline{R}$	Write/Read Input
$\overline{ADS}$	CPU Address Strobe Input
$\overline{EADS}$	External Address Strobe Input
TAG_0-TAG_8	Tag Data Input/Output
$\overline{TWE}$	Tag Write Input
$\overline{TCE}$	Tag Chip Enable Input
PD_0-PD_2	Presence Detect Pins
NC	No Connection

Presence Detect Table

	PD_2	PD_1	PD_0
CYM7424	NC	V_{CC}	NC
CYM7425	NC	NC	V_{CC}

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −55°C to +125°C

Ambient Temperature with Power Applied ..... −0°C to +70°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CYM7424 CYM7425		Unit
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = 4 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}+0.3	V
V_{IL}	Input LOW Voltage		−0.5	0.8	V
I_{CC}	V_{CC} Operating Supply Current (CYM7424 only.)	V_{CC} = Max., I_{OUT} = 0 mA		1250	mA
I_{CC}	V_{CC} Operating Supply Current (CYM7425 only.)	V_{CC} = Max., I_{OUT} = 0 mA		1850	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current (CYM7424)	Max. V_{CC}, CS $\geq V_{IH}$, f=fmax $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$		550	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current (CYM7425)	Max. V_{CC}, CS $\geq V_{IH}$, f=0 $V_{IN} \geq V_{CC}$ −0.3V or $V_{IN} \leq$ 0.3V		360	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, CS $\geq V_{IH}$, f=fmax $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$		800	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, CS $\geq V_{IH}$, f=0 $V_{IN} \geq V_{CC}$ −0.3V or $V_{IN} \leq$ 0.3V		420	mA

Ordering Information

Cache Memory Size	Ordering Code	Package Name	Package Type	Operating Range
128 Kbyte	CYM7424PB−20C	PM11	112-Pin Dual-Readout SIMM	Commercial
256 Kbyte	CYM7425PB−20C	PM12	112-Pin Dual-Readout SIMM	Commercial

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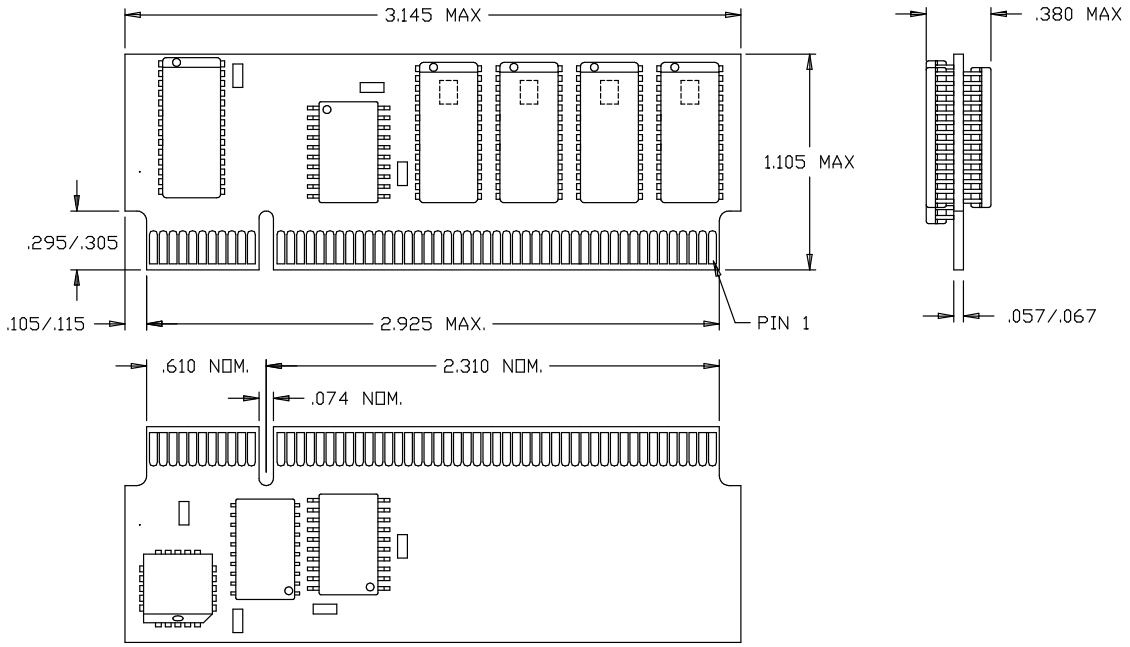
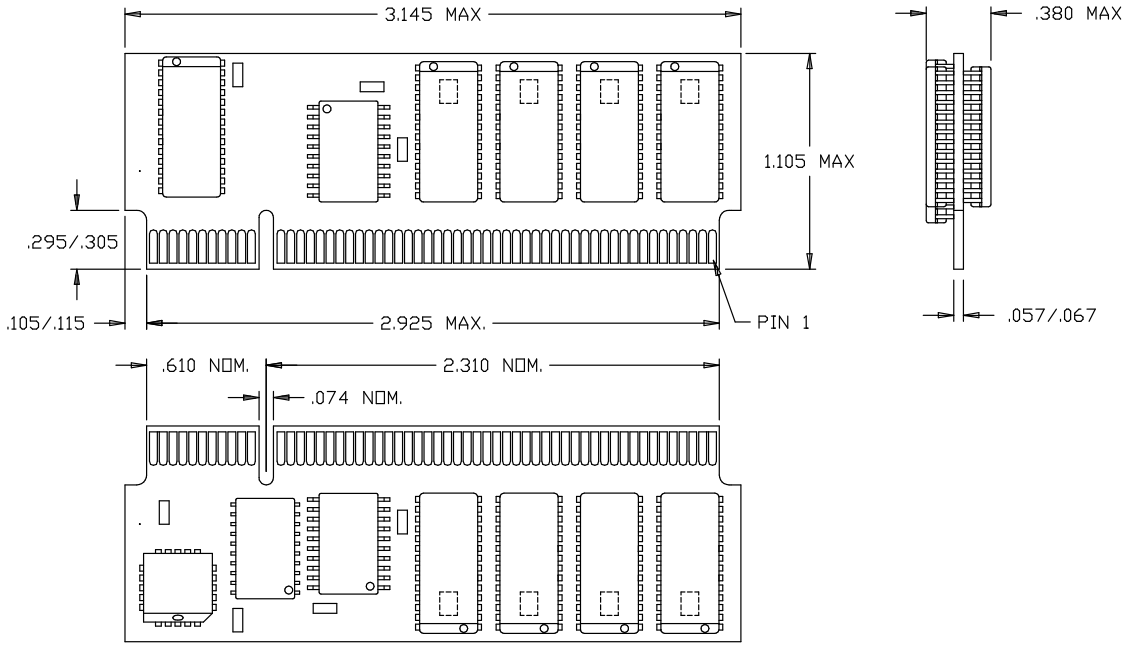
Package Diagram

112-Pin Dual-Readout SIMM PM11



112-Pin Dual-Readout SIMM PM12



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