*PRELIMINARY*

# CYM7490
# CYM7491
# CYM7492

## i486 Level II Cache Module Family

### Features

- **Cache sizes of 64 KB, 256 KB, or 1 MB**
- **Tag width of 8 bits**
- **Independent dirty bit**
- **Operates with 33-MHz Intel i486 processors**
- **Zero-wait-state operation**
- **Constructed using standard asynchronous SRAMs**
- **64-position (128-signal) dual-readout SIMM**
- **Single 5V (±5%) power supply**
- **TTL-compatible inputs/outputs**

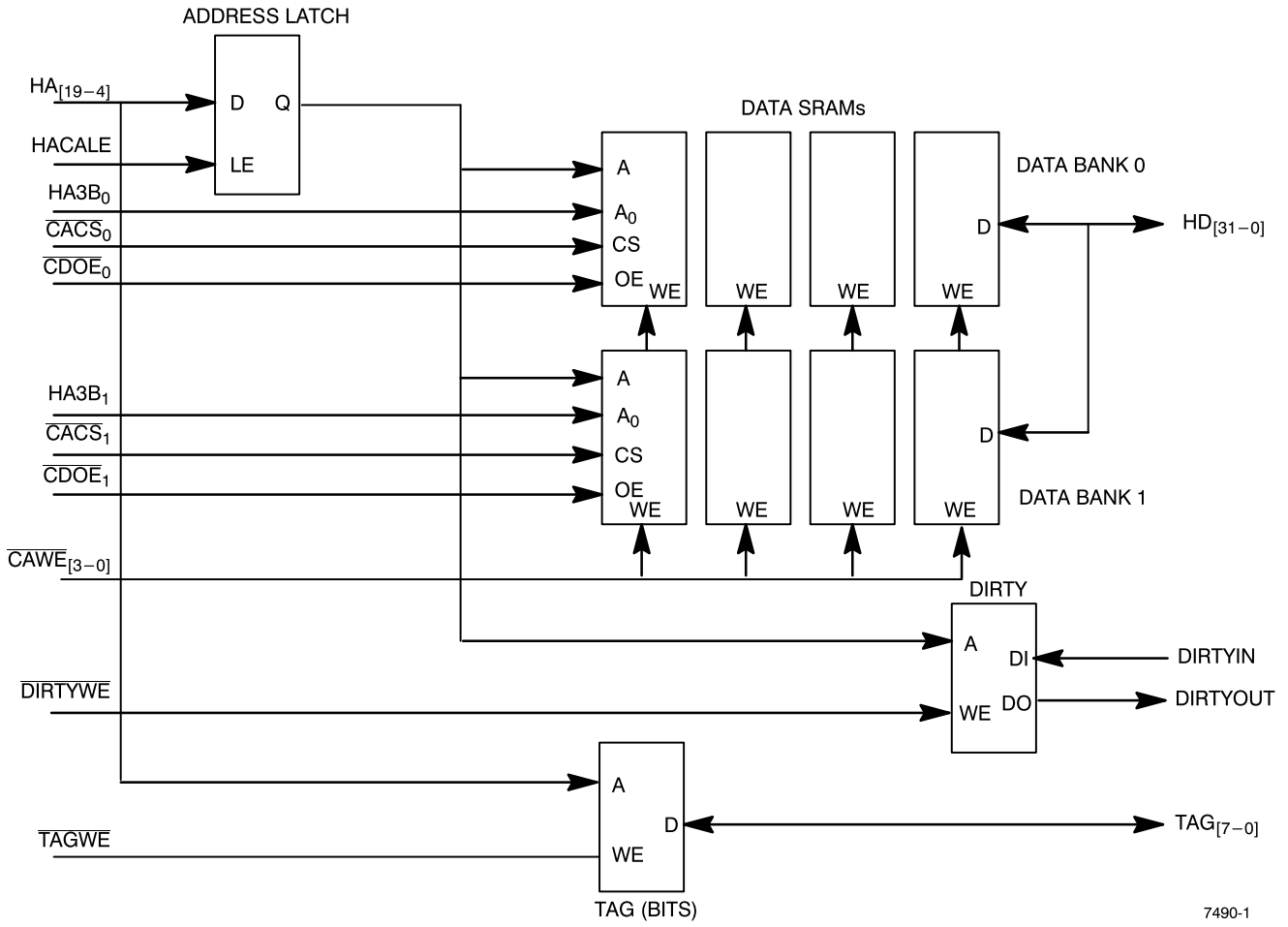
### Functional Description

The CYM7490 module series is a family of cache memory subsystems for Intel i486-based systems. Each module contains two banks of 32-bit-wide data SRAM, an 8-bit-wide tag SRAM, and a single-bit-wide, separate I/O dirty SRAM. Bank sizes of 8K x 32, 32K x 32, and 128K x 32 are supported, yielding cache sizes of 64 kilobytes, 256 kilobytes, and 1 megabyte. The address signals for the data and dirty SRAMs are latched.

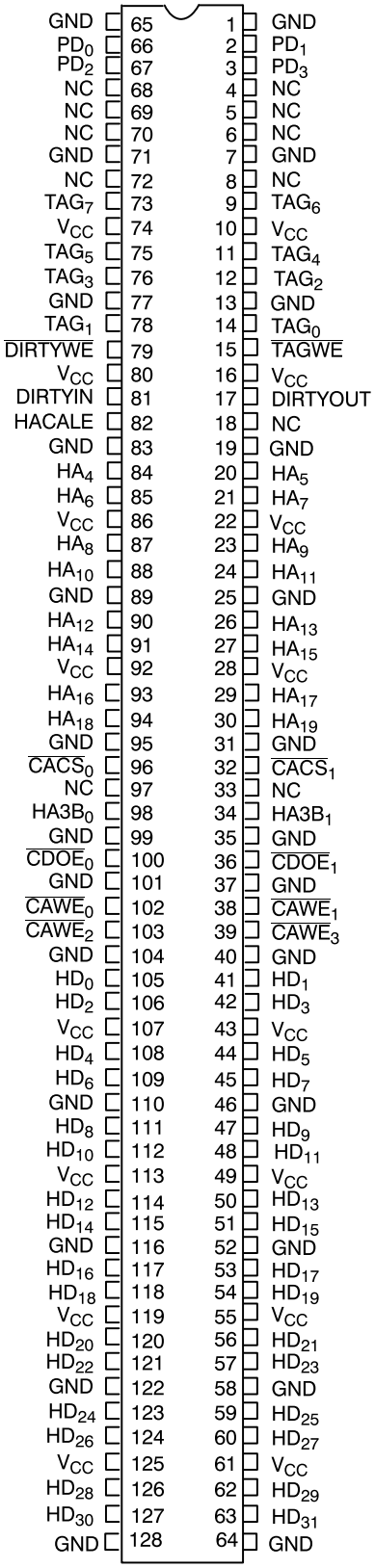
The module is configured as a 128-pin dual-readout single-in-line memory module (SIMM). It is constructed using standard asynchronous SRAMs in SOJ packages mounted on an epoxy laminate substrate. The SIMM contacts are plated with five micro-inches of gold over 100 micro-inches of nickel. Module dimensions are 3.85 inches long by 1.15 inches high by 0.33 inches thick.

These modules are designed for zero-wait-state operation in 486-based systems operating at a bus speed of 33 MHz. They are designed for compatibility with off-the-shelf cache controllers and chipsets. The 15-ns device is built using data and tag SRAMs with an access time of 15 ns, while the 20-ns version is built with 15-ns tag SRAMs and 20-ns data SRAMs.

### Logic Block Diagram



**Dual-Readout SIMM**
**Top View**




7490-2

## Signal Descriptions

| Signal | Type | Description |
|---|---|---|
| $TAG_{7-0}$ | I/O | Cache Tag Data Bus |
| $\overline{TAGWE}$ | I | Tag Write Enable |
| $\overline{DIRTYWE}$ | I | Dirty Bit Write Enable |
| DIRTYIN | I | Dirty Bit In |
| DIRTYOUT | O | Dirty Bit Out |
| HACALE | I | Host Address Bus Latch Enable |
| $HA_{19-4}$ | I | Host Address Bus. |
| $\overline{CACS}_{1-0}$ | I | Cache Memory Chip Selects |
| $HA3B_{1-0}$ | I | Host Address A3 Bank Select |
| $\overline{CDOE}_{1-0}$ | I | Cache Data Output Enable |
| $\overline{CAWE}_{3-0}$ | I | Cache Write Enables |
| $HD_{31-0}$ | I/O | Host Data Bus |
| $PD_{3-0}$ | O | Presence Detect Pins (see below) |
| NC | – | Reserved for future use. |

## Presence Detect Scheme

| **Device** | **$PD_3$** | **$PD_2$** | **$PD_1$** | **$PD_0$** |
|---|---|---|---|---|
| CYM7490 | Open | Open | Open | GND |
| CYM7491 | Open | Open | GND | Open |
| CYM7492 | Open | Open | GND | GND |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −55°C to +150°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... −0.5V to +7.0V

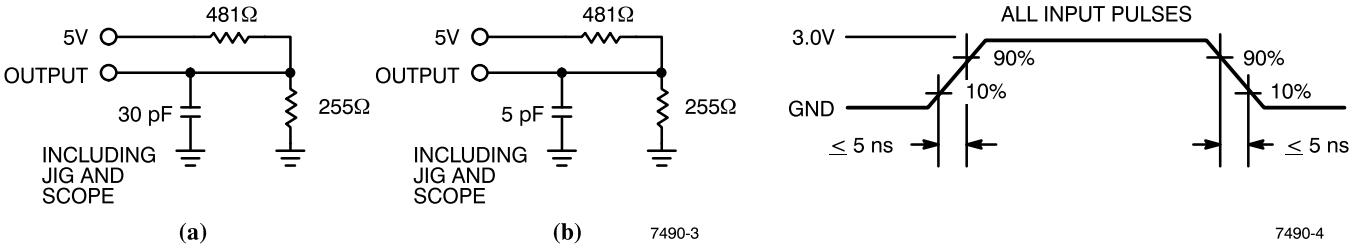
## Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | CYM7490−15, 20 CYM7491−15, 20 CYM7492−15, 20 Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | 4.5 | 5.5 | V |
| $T_{AMB}$ | Ambient Temperature | Commercial | 0 | 70 | °C |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min. $I_{OH}$ = −4.0 mA | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min. $I_{OL}$ = 8..0 mA | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage Level | | 2.2 | $V_{CC}$ | V |
| $V_{IL}$ | Input LOW Voltage Level | | −0.5 | 0.8 | V |
| $L_{IN}$ | Input Leakage Output | $V_{CC}$ = Max., $0 \le V_{IN} \le V_{SS}$ | | ±20 | µA |
| $I_{OUT}$ | Operating Leakage Current | $\overline{CS}$=$V_{IH}$, $V_{CC}$ =Max., $V_{SS} \le V_{OUT} \le V_{CC}$ | | ±20 | µA |
| $I_{CC1}$ | Operating Current | $\overline{CACSn}$ = $V_{IL}$, Outputs Open, f=$f_{MAX}$ | | 1300 | mA |
| $I_{SB1}$ | Standby Current − TTL Levels | $\overline{CACSn} \ge V_{CC}$ −0.2, $V_{CC}$ = Max., $V_{CC}$ −0.2 ≤ $V_{IN}$ ≤ 0.2, Outputs Open | | 800 | mA |
| $I_{SB2}$ | Standby Current − CMOS Levels | $\overline{CACSn} \ge V_{CC}$ −0.2, $V_{CC}$ = Max., $V_{CC}$−0.2 ≤$V_{IN}$≤ 0.2, Outputs Open | | 400 | mA |

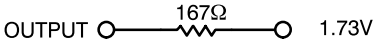
## Capacitance

| Parameter | Description | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{ADDR}$ | Input Capacitance, $HA_{19-4}$, $CAA3_{1-0}$ | f=1 MHz | 50 | pF |
| $C_{WE}$ | Input Capacitance, $\overline{CAWE}_{1-0}$, $\overline{TAGWE}$ | f=1 MHz | 30 | pF |
| $C_{WE2}$ | Input Capacitance, $\overline{DIRTYWE}$, HACALE | f=1 MHz | 20 | pF |
| $C_{CSOE}$ | Input Capacitance, $\overline{CACS}_{1-0}$, $\overline{CDOE}_{1-0}$ | f=1 MHz | 50 | pF |
| $C_{DATA}$ | Input/Output Capacitance, $HD_{31-0}$ | f=1 MHz | 90 | pF |
| $C_{TAG}$ | Input/Output Capacitance, $TAG_{7-0}$, DIRTYIN, DIRTYOUT | f=1 MHz | 30 | pF |

## AC Test Loads and Waveforms




Equivalent to: THÉVENIN EQUIVALENT



**Switching Characteristics** Over the Operating Range

| Parameter | Description | 7490−15 7491−15 7492−15 | | 7490−20 7491−20 7492−20 | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| **ADDRESS LATCH** | | | | | | |
| $t_{LPW}$ | Latch Pulse Width | 5 | | 5 | | ns |
| $t_{LSD}$ | Data Set-Up to ALE Positive | 2 | | 2 | | ns |
| $t_{LHD}$ | Data Hold from ALE Positive | 1.5 | | 1.5 | | ns |
| **READ CYCLE − Data SRAM Read Timing** | | | | | | |
| $t_{RC}$ | Read Cycle Time | 20 | | 25 | | ns |
| $t_{AA}$ | Address Access Time (Latch Transparent) | | 20 | | 25 | ns |
| $t_{OE}$ | Output Enable to Output Valid | | 10 | | 10 | ns |
| $t_{CE}$ | Chip Enable to Data Valid | | 15 | | 20 | ns |
| $t_{OHA}$ | Data Hold After Address Change | 3 | | 3 | | ns |
| $t_{LZCE}$ | Chip Enable to Outputs in Low Z | 3 | | 3 | | ns |
| $t_{HZCE}$ | Chip Disable to Outputs in High Z | | 8 | | 10 | ns |
| $t_{OLZ}$ | Output Enable to Outputs in Low Z | 0 | | 0 | | ns |
| $t_{OHZ}$ | Output Disable to Outputs in High Z | | 8 | | 10 | ns |
| **READ CYCLE − Tag SRAM Read Timing** | | | | | | |
| $t_{TDRC}$ | Read Cycle Time | 15 | | 20 | | ns |
| $t_{TAA}$ | Address Access Time | | 15 | | 20 | ns |
| $t_{TCE}$ | Chip Enable to Data Valid | | 15 | | 20 | ns |
| $t_{TOHA}$ | Data Hold After Address Change | 3 | | 3 | | ns |
| $t_{TLZCE}$ | Chip Enable to Outputs in Low Z | 3 | | 3 | | ns |
| $t_{THZCE}$ | Chip Disable to Outputs in High Z | | 8 | | 8 | ns |
| **READ CYCLE − Dirty SRAM Read Timing** | | | | | | |
| $t_{DRC}$ | Read Cycle Time | 20 | | 25 | | ns |
| $t_{DAA}$ | Address Time | | 20 | | 25 | ns |
| $t_{DOHA}$ | Data Hold After Address Change | 3 | | 3 | | ns |
| **WRITE CYCLE − Data SRAM Write Timing** | | | | | | |
| $t_{WC}$ | Write Cycle Time | 20 | | 25 | | ns |
| $t_{SCE}$ | Chip Enable to End of Write | 10 | | 15 | | ns |
| $t_{AW}$ | Address Set-Up to End of Write | 20 | | 25 | | ns |
| $t_{AH}$ | Address Hold from End of Write | 0 | | 0 | | ns |
| $t_{SA}$ | Address Set-Up from Beginning of Write | 5 | | 5 | | ns |
| $t_{PWE}$ | Write Pulse Width | 10 | | 15 | | ns |
| $t_{SD}$ | Data Set-Up to End of Write | 7 | | 10 | | ns |
| $t_{HD}$ | Data Hold from End of Write | 0 | | 0 | | ns |
| $t_{LZWE}$ | Write HIGH to Outputs in Low Z | 3 | | 3 | | ns |
| $t_{HZWE}$ | Write LOW to Outputs in High Z | | 7 | | 10 | ns |

## Switching Characteristics (continued)

| Parameter | Description | 7490−15 7491−15 7492−15 | | 7490−20 7491−20 7492−20 | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| **WRITE CYCLE − Tag SRAM Write Timing** | | | | | | |
| $t_{TWC}$ | Write Cycle Time | 15 | | 15 | | ns |
| $t_{TSCE}$ | Chip Enable to End of Write | 10 | | 10 | | ns |
| $t_{TAW}$ | Address Set-Up to End of Write | 10 | | 10 | | ns |
| $t_{TAH}$ | Address Hold from End of Write | 0 | | 0 | | ns |
| $t_{TSA}$ | Address Set-Up from Beginning of Write | 0 | | 0 | | ns |
| $t_{TPWE}$ | Write Pulse Width | 10 | | 10 | | ns |
| $t_{TSD}$ | Data Set-Up to End of Write | 7 | | 7 | | ns |
| $t_{THD}$ | Data Hold from End of Write | 0 | | 0 | | ns |
| $t_{TLZWE}$ | Write HIGH to Outputs in Low Z | 3 | | 3 | | ns |
| $t_{THZWE}$ | Write LOW to Outputs in High Z | | 7 | | 7 | ns |
| **WRITE CYCLE − Dirty SRAM Write Timing** | | | | | | |
| $t_{DWC}$ | Write Cycle Time | 20 | | 20 | | ns |
| $t_{DAW}$ | Address Set-Up to End of Write | 17 | | 17 | | ns |
| $t_{DAH}$ | Address Hold from End of Write | 0 | | 0 | | ns |
| $t_{DSA}$ | Address Set-Up from Beginning of Write | 5 | | 5 | | ns |
| $t_{DPWE}$ | Write Pulse Width | 12 | | 12 | | ns |
| $t_{DSD}$ | Data Set-Up to End of Write | 10 | | 10 | | ns |
| $t_{DHD}$ | Data Hold from End of Write | 0 | | 0 | | ns |
| $t_{DLZWE}$ | Write HIGH to Outputs in Low Z | 5 | | 5 | | ns |
| $t_{DHZWE}$ | Write LOW to Outputs in High Z | | 7 | | 7 | ns |

## Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Cache Size |
|---|---|---|---|---|
| 15 (Data and Tag/Dirty) | CYM7490PM−15 | PM05 | 128-Pin Dual-Readout SIMM | 64 Kbyte |
| 20 (Data), 15 (Tag/Dirty) | CYM7490PM−20 | PM05 | 128-Pin Dual-Readout SIMM | |

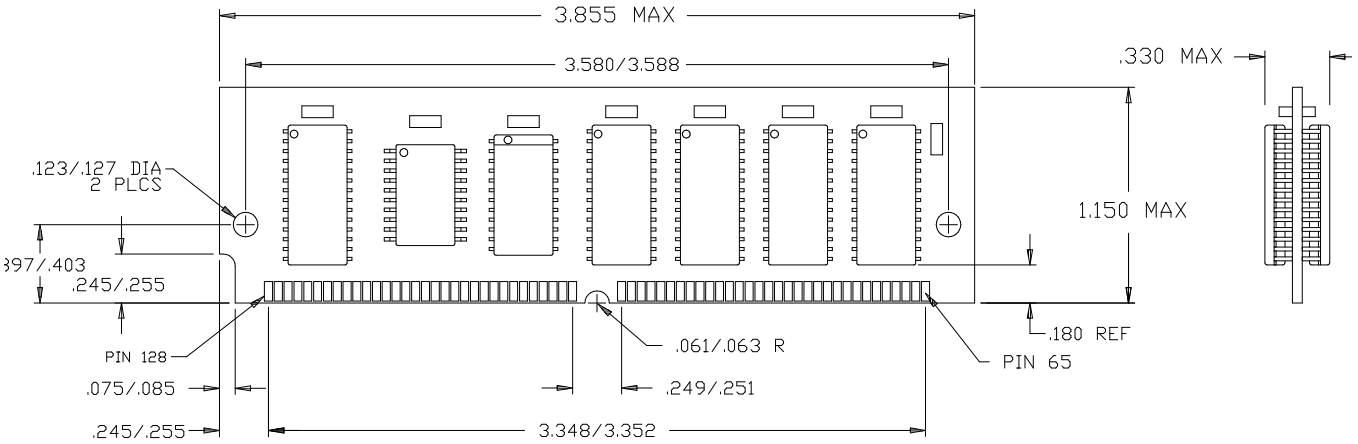
| Speed (ns) | Ordering Code | Package Name | Package Type | Cache Size |
|---|---|---|---|---|
| 15 (Data and Tag/Dirty) | CYM7491PM−15 | PM06 | 128-Pin Dual-Readout SIMM | 256 Kbyte |
| 20 (Data), 15 (Tag/Dirty) | CYM7491PM−20 | PM06 | 128-Pin Dual-Readout SIMM | |

| Speed (ns) | Ordering Code | Package Name | Package Type | Cache Size |
|---|---|---|---|---|
| 15 (Data and Tag/Dirty) | CYM7492PM−15 | PM07 | 128-Pin Dual-Readout SIMM | 1 Mbyte |
| 20 (Data), 15 (Tag/Dirty) | CYM7492PM−20 | PM07 | 128-Pin Dual-Readout SIMM | |

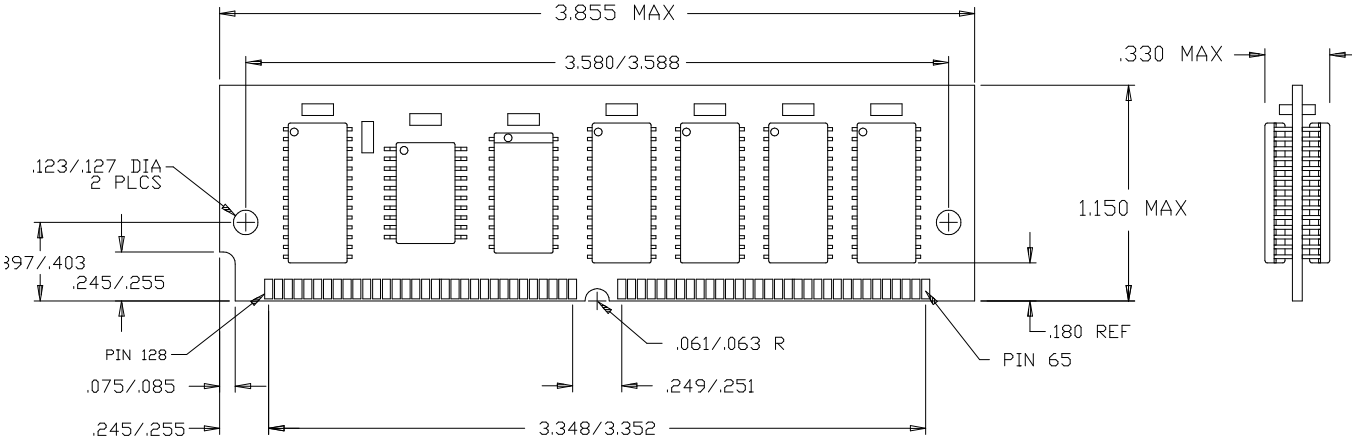
Document #: 38−M−00061

## Package Diagrams

**128-Pin Dual-Readout SIMM Module PM05**




**128-Pin Dual-Readout SIMM Module PM06**




**128-Pin Dual-Readout SIMM Module PM07**