# CYM74A550, CYM74A551
*PRELIMINARY* **CYM74S550, CYM74S551**

# OPTi Viper™ Chip Set Level II Cache Module Family

## Features

- **Pin-compatible secondary cache module family**
- **Asynchronous (CYM74A550, CYM74A551) or synchronous (CYM74S550, CYM74S551) modules with presence and configuration detect pins**
- **Ideal for Intel P54C-based systems with the OPTi Viper™ chipset**
- **Operates at 50, 60, and 66 MHz**
- **Uses cost-effective CMOS asynchronous SRAMs or high-performance synchronous SRAMs**
- **160-position Burndy DIMM CELP2X80SC3Z48 connector**
- **3.3V inputs/outputs**

## Functional Description

This family of secondary cache modules is designed for Intel P54C systems with the OPTi Viper chip set.

CYM74A550 and CYM74A551 are low-cost asynchronous cache modules that provide 256-Kbytes and 512-Kbytes of cache respectively. These modules offer 3-2-2-2 performance at CPU bus speeds up to 66 MHz.

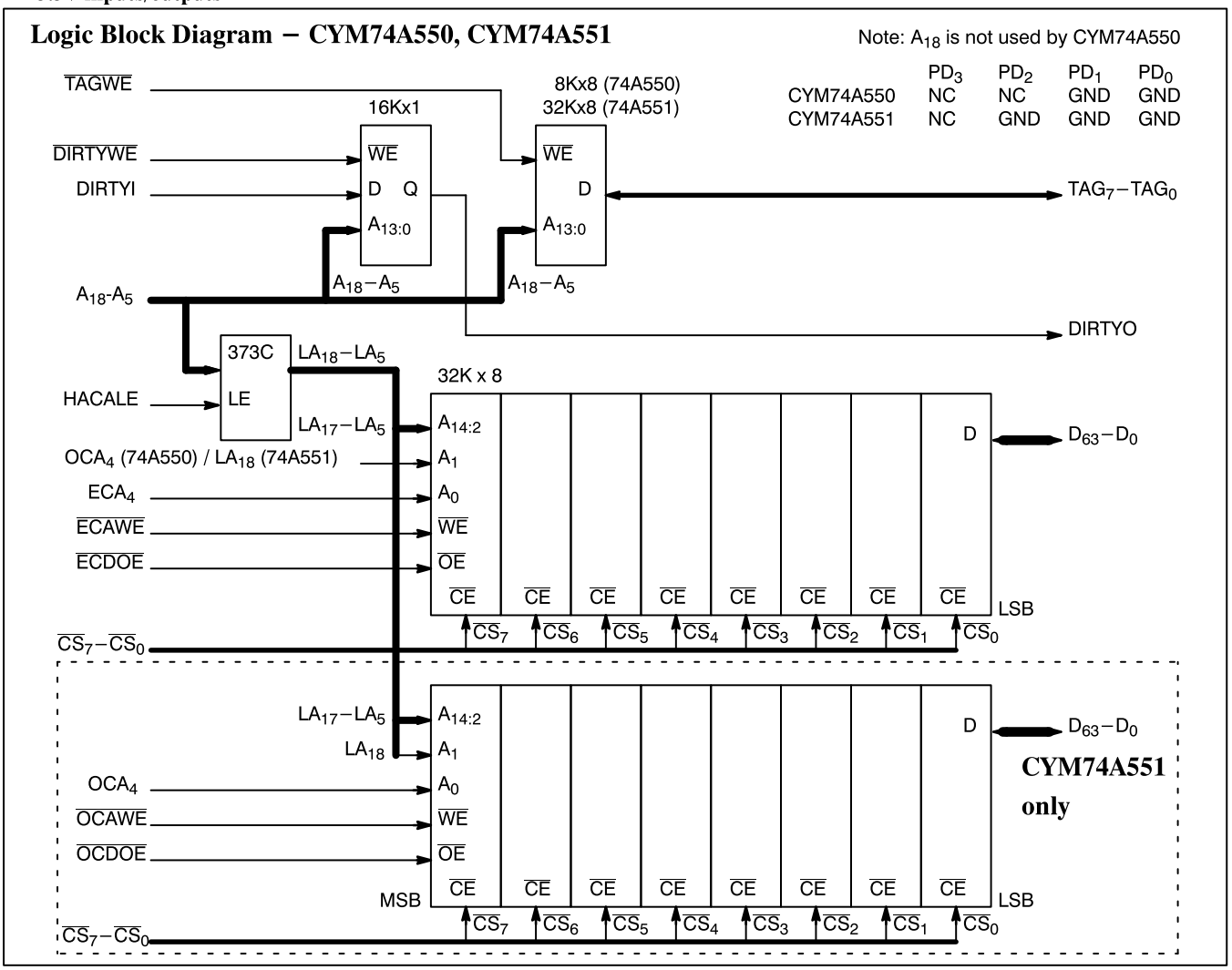
The CYM74S550 and CYM74S551 are high performance synchronous cache modules that provide 256-Kbytes and 512-Kbytes of cache respectively. These modules support 3-1-1-1 performance at 66 MHz.

All of these modules include storage for 8 bits of tag and one dirty bit.

Multiple ground pins and on-board decoupling capacitors ensure high performance with maximum noise immunity.

All components on the cache modules are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. All inputs and outputs of this family of modules are (3.3V) TTL compatible. Provisions are made on-board to support both mixed-mode (5V/3.3V) and 3.3V-only SRAMs. The contact pins are plated with 100 micro-inches of nickel covered by 10 micro-inches of gold flash.

## Logic Block Diagram – CYM74A550, CYM74A551

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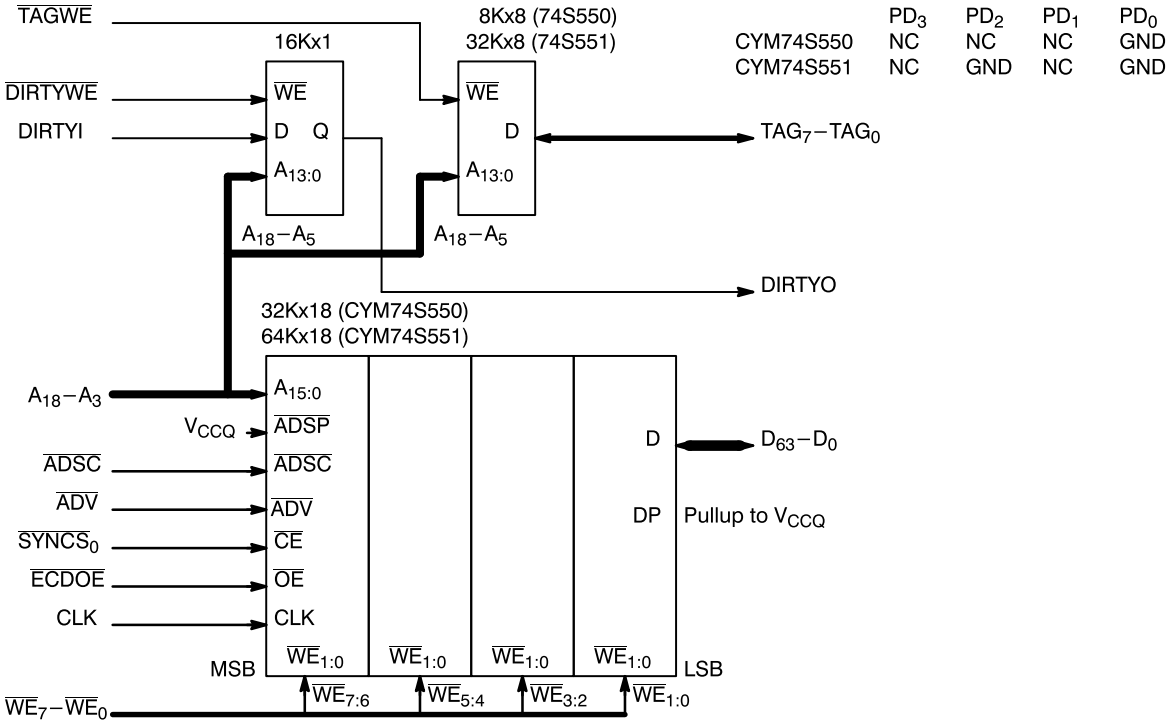
## Logic Block Diagram – CYM74S550, CYM74S551

Note: $A_{18}$ is not used by CYM74S550




| | PD3 | PD2 | PD1 | PD0 |
|---|---|---|---|---|
| CYM74S550 | NC | NC | NC | GND |
| CYM74S551 | NC | GND | NC | GND |

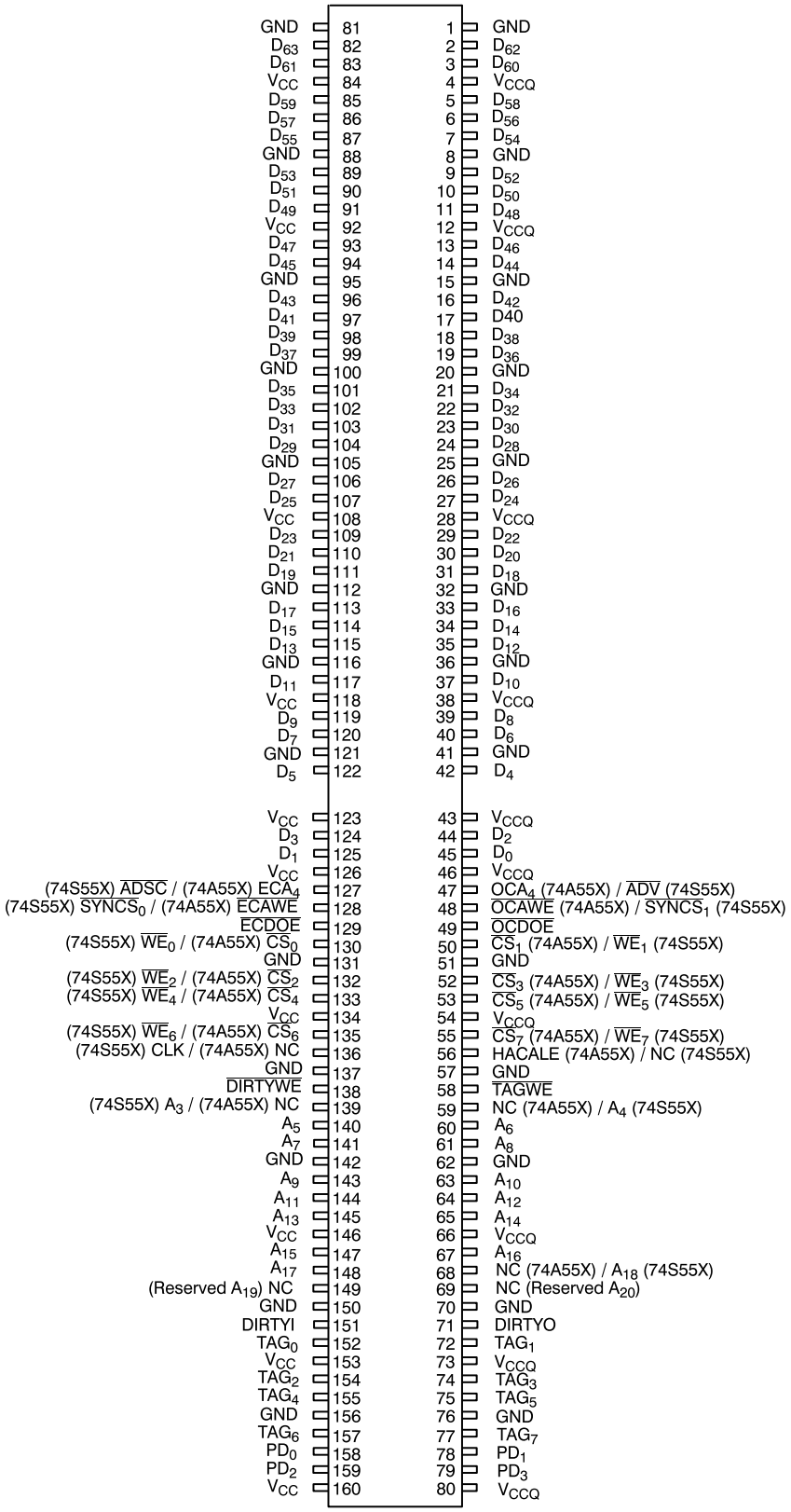
## Selection Guide

| | Asynchronous Cache Modules | | | | | |
|---|---|---|---|---|---|---|
| **Part Number** | **74A550–50** | **74A550–60** | **74A550–66** | **74A551–50** | **74A551–60** | **74A551–66** |
| Cache Size | 256 KB | | | 512 KB | | |
| System Clock (MHz) | 50 | 60 | 66 | 50 | 60 | 66 |
| Data $t_{AA}$ | 25 ns | 15 ns | 15 ns | 25 ns | 15 ns | 15 ns |
| Tag $t_{AA}$ | 20 ns | 15 ns | 12 ns | 20 ns | 15 ns | 12 ns |

| | Synchronous Cache Modules | | | | | |
|---|---|---|---|---|---|---|
| **Part Number** | **74S550–50** | **74S550–60** | **74S550–66** | **74S551–50** | **74S551–60** | **74S551–66** |
| Cache Size | 256 KB | | | 512 KB | | |
| System Clock (MHz) | 50 | 60 | 66 | 50 | 60 | 66 |
| Data $t_{CDV}$ | 12 ns | 9 ns | 9 ns | 12 ns | 9 ns | 9 ns |
| Tag $t_{AA}$ | 20 ns | 15 ns | 12 ns | 20 ns | 15 ns | 12 ns |

## Pin Configuration

**Dual Read-Out SIMM (DIMM)**
**Top View**



## Pin Definitions

| Common Signals | Description |
|---|---|
| $V_{CC}$ | 5V Supply |
| $V_{CCQ}$ | 3.3V Supply |
| GND | Ground |
| $A_{18}-A_5$ | Addresses from processor |
| $D_{63}-D_0$ | 64-bit Data bus from processor |
| $\overline{ECDOE}$ | Even bank output enable input |
| $TAG_7-TAG_0$ | 8-bit Tag RAM bidirectional bus |
| $\overline{TAGWE}$ | Tag RAM write enable input |
| DIRTYI | 1-bit Dirty RAM input |
| DIRTYO | 1-bit Dirty RAM output |
| $\overline{DIRTYWE}$ | Dirty RAM write enable input |
| $PD_3-PD_0$ | Presence Detect pins |
| NC | Signal not connected on module. |
| **CYM74A55X Only Signals** | **Description** |
| HACALE | Address Latch Enable input to transparent address latches |
| $OCA_4$ | Address bit $A_3$ in single bank async cache module (CYM74A550)<br>Address bit $A_4$ of odd bank in two bank async cache module (CYM74A551) |
| $ECA_4$ | Address bit $A_4$ in single bank async cache module (CYM74A550)<br>Address bit $A_4$ of even bank in two bank async cache module (CYM74A551) |
| $\overline{CS}_7-\overline{CS}_0$ | Data RAM Chip Select inputs |
| $\overline{ECAWE}$ | Even bank write enable input |
| $\overline{OCAWE}$ | Odd bank write enable input (CYM74A551 only) |
| **CYM74S55X Only Signals** | **Description** |
| CLK | Clock input |
| $A_4-A_3$ | Lower order address bits from processor |
| $\overline{ADSC}$ | Cache Controller Address Strobe input |
| $\overline{ADV}$ | Burst Address Advance input |
| $\overline{SYNCS_0}$ | Even bank synchronous burst RAM chip select input |
| $\overline{SYNCS_1}$ | Odd bank synchronous burst RAM chip select input (not used) |
| $\overline{WE}_7-\overline{WE}_0$ | Write enable inputs to Data RAMs |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −55°C to +125°C

Ambient Temperature with Power Applied ..... −0°C to +70°C

3.3V Supply Voltage to Ground Potential .... −0.5V to +4.6V

5V Supply Voltage to Ground Potential ..... −0.5V to +5.25V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +4.6V

DC Input Voltage ..... −0.5V to +4.6V

Output Current into Outputs (LOW) ..... 20 mA

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to +70°C | 5V ± 5% 3.3V ± 5% |

## Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.2 | $V_{CCQ}$ + 0.3 | V |
| $V_{IL}$ | Input LOW Voltage | | −0.3 | 0.8 | V |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$=Min. $I_{OH}$ = −4 mA | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$=Min. $I_{OL}$ = 8 mA | | 0.4 | V |
| $I_{CC}$ (74A550) | $V_{CC}$ Operating Supply Current | $V_{CC}$=Max., $I_{OUT}$=0 mA, f=$f_{MAX}$=1/$t_{RC}$ | | 1500 | mA |
| $I_{CC}$ (74A551) | $V_{CC}$ Operating Supply Current | $V_{CC}$=Max., $I_{OUT}$=0 mA, f=$f_{MAX}$=1/$t_{RC}$ | | 2700 | mA |
| $I_{CC}$ (74S550) | $V_{CC}$ Operating Supply Current | $V_{CC}$=Max., $I_{OUT}$=0 mA, f=$f_{MAX}$=1/$t_{RC}$ | | 1500 | mA |
| $I_{CC}$ (74S551) | $V_{CC}$ Operating Supply Current | $V_{CC}$=Max., $I_{OUT}$=0 mA, f=$f_{MAX}$=1/$t_{RC}$ | | 1500 | mA |

## Ordering Information

| Speed (MHz) | Ordering Code | Package Name | Package Type | Description | Operating Range |
|---|---|---|---|---|---|
| 50 | CYM74A550PM−50C | PM31 | 160-Pin Dual-Readout SIMM | Async 256 KB | Commercial |
| | CYM74A551PM−50C | PM32 | | Async 512 KB | |
| | CYM74S550PM−50C | PM33 | | Sync 256 KB | |
| | CYM74S551PM−50C | PM33 | | Sync 512 KB | |
| 60 | CYM74A550PM−60C | PM31 | 160-Pin Dual-Readout SIMM | Async 256 KB | Commercial |
| | CYM74A551PM−60C | PM32 | | Async 512 KB | |
| | CYM74S550PM−60C | PM33 | | Sync 256 KB | |
| | CYM74S551PM−60C | PM33 | | Sync 512 KB | |
| 66 | CYM74A550PM−66C | PM31 | 160-Pin Dual-Readout SIMM | Async 256 KB | Commercial |
| | CYM74A551PM−66C | PM32 | | Async 512 KB | |
| | CYM74S550PM−66C | PM33 | | Sync 256 KB | |
| | CYM74S551PM−66C | PM33 | | Sync 512 KB | |

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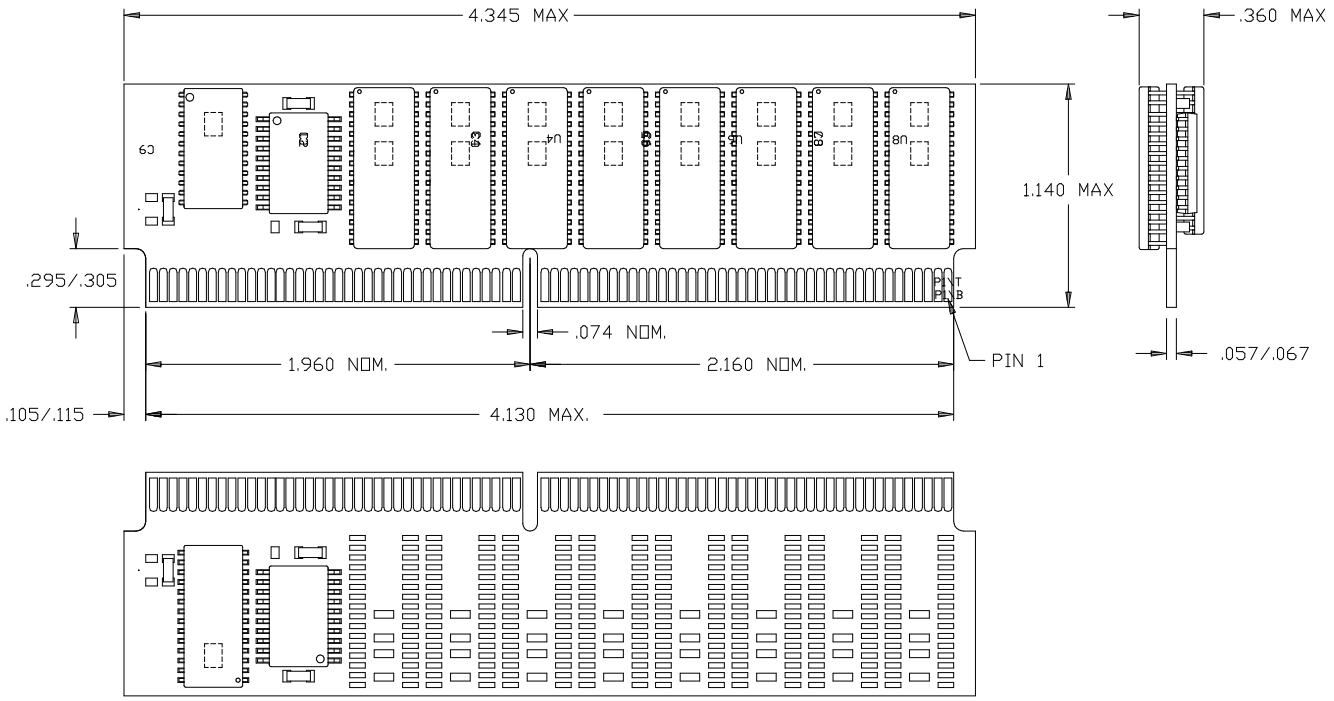
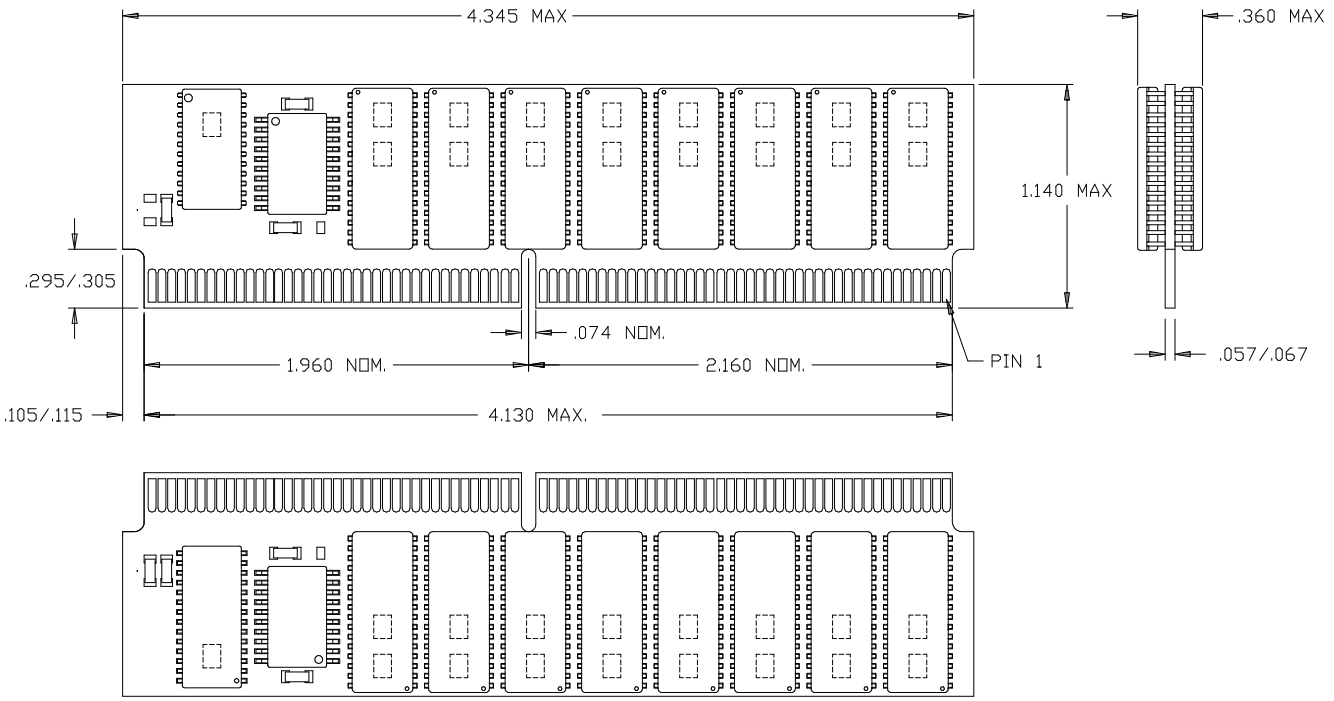
## Package Diagrams

**160-Pin Dual Readout SIMM PM31**




**160-Pin Dual Readout SIMM PM32**



## Package Diagrams (continued)

**160-Pin Dual Readout SIMM PM33**