PRELIMINARY

CYM74AP54
CYM74SP54
CYM74SP55

Intel™ 82430NX Chip Set Level II Cache Module Family

Features

- **Pin-compatible secondary cache module family**
- **Asynchronous (CYM74AP54) or synchronous (CYM74SP54, CYM74SP55) configurations with presence and configuration detect pins**
- **Ideal for Intel P54C-based systems with the 82430NX (Neptune) chip set**
- **Operates at 60 and 66 MHz**
- **Uses cost-effective CMOS asynchronous SRAMs or high-performance synchronous SRAMs**
- **160-position Burndy DIMM CELP2X80SC3Z48 connector**
- **3.3V inputs/outputs**

Functional Description

This family of secondary cache modules is designed for Intel P54C systems with the 82430NX (Neptune) chip set.

CYM74AP54 is an asynchronous 256-Kbyte cache module that provides a low-cost, high-performance solution for CPU bus speeds up to 66 MHz. The CYM74AP54 is organized as 32K by 64.

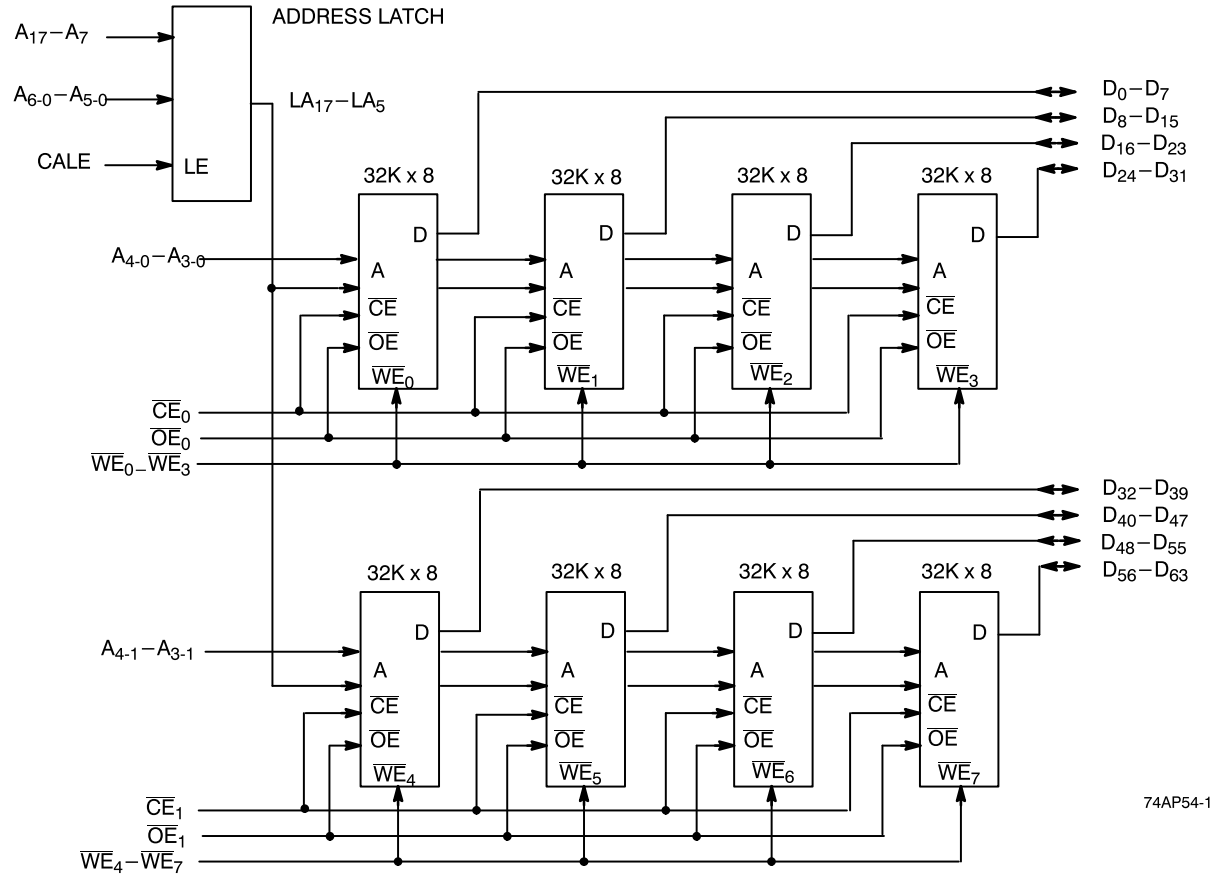
The CYM74SP54 and CYM74SP55 are synchronous cache modules that provide zero wait-state performance at a bus speed of 66 MHz. The CYM74SP54 is a 256-Kbyte cache module with byte parity.

The CYM74SP55 is a 512-Kbyte cache module with byte parity.

Multiple ground pins and on-board decoupling capacitors ensure high performance with maximum noise immunity.

All components on the cache modules are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. All inputs and outputs of this family of modules are (3.3V) TTL compatible. Provisions are made on-board to support both mixed−mode (5V/3.3V) and 3.3V only SRAMs. The contact pins are plated with 100 micro-inches of nickel covered by 10 micro-inches of gold flash.

Logic Block Diagram − CYM74AP54



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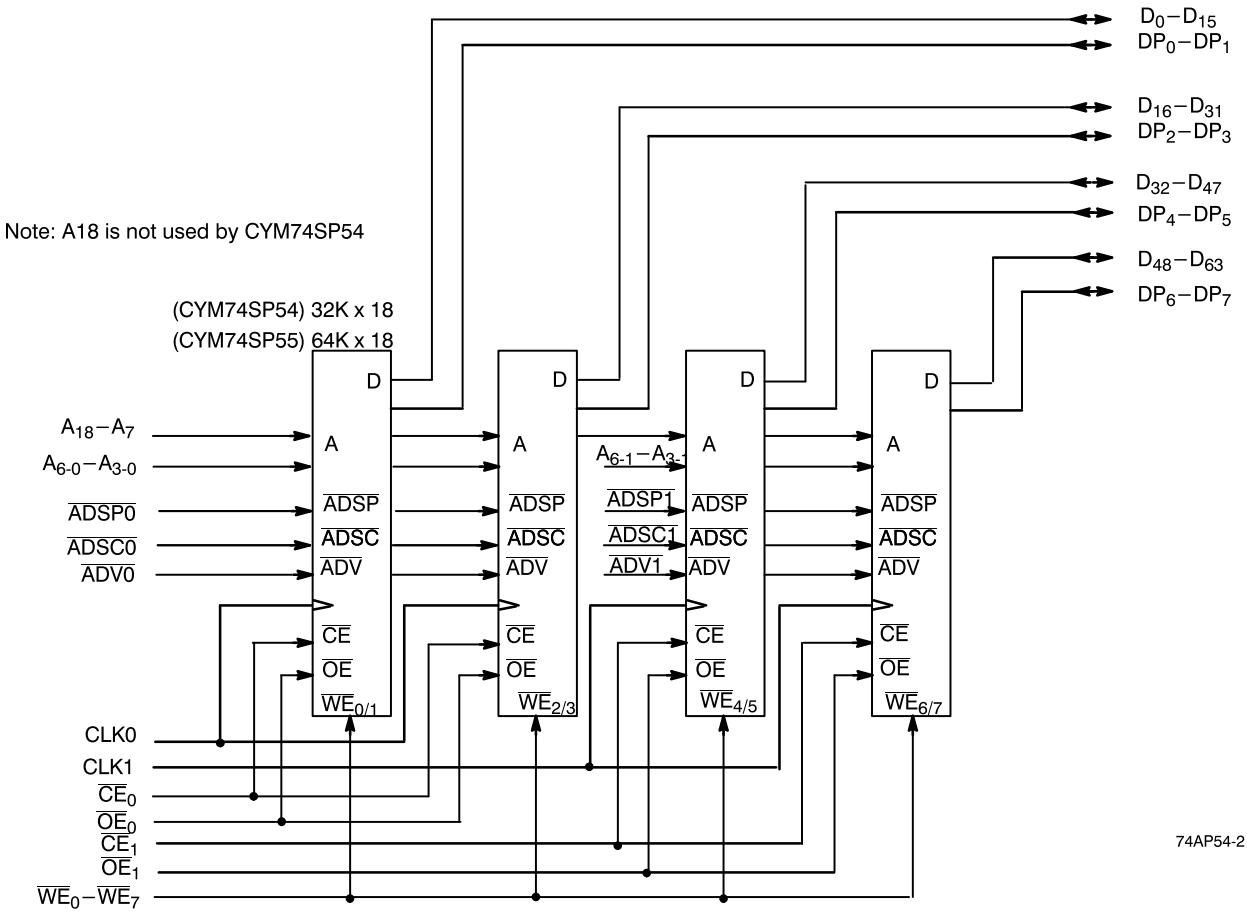
Logic Block Diagram − CYM74SP54/CYM74SP55

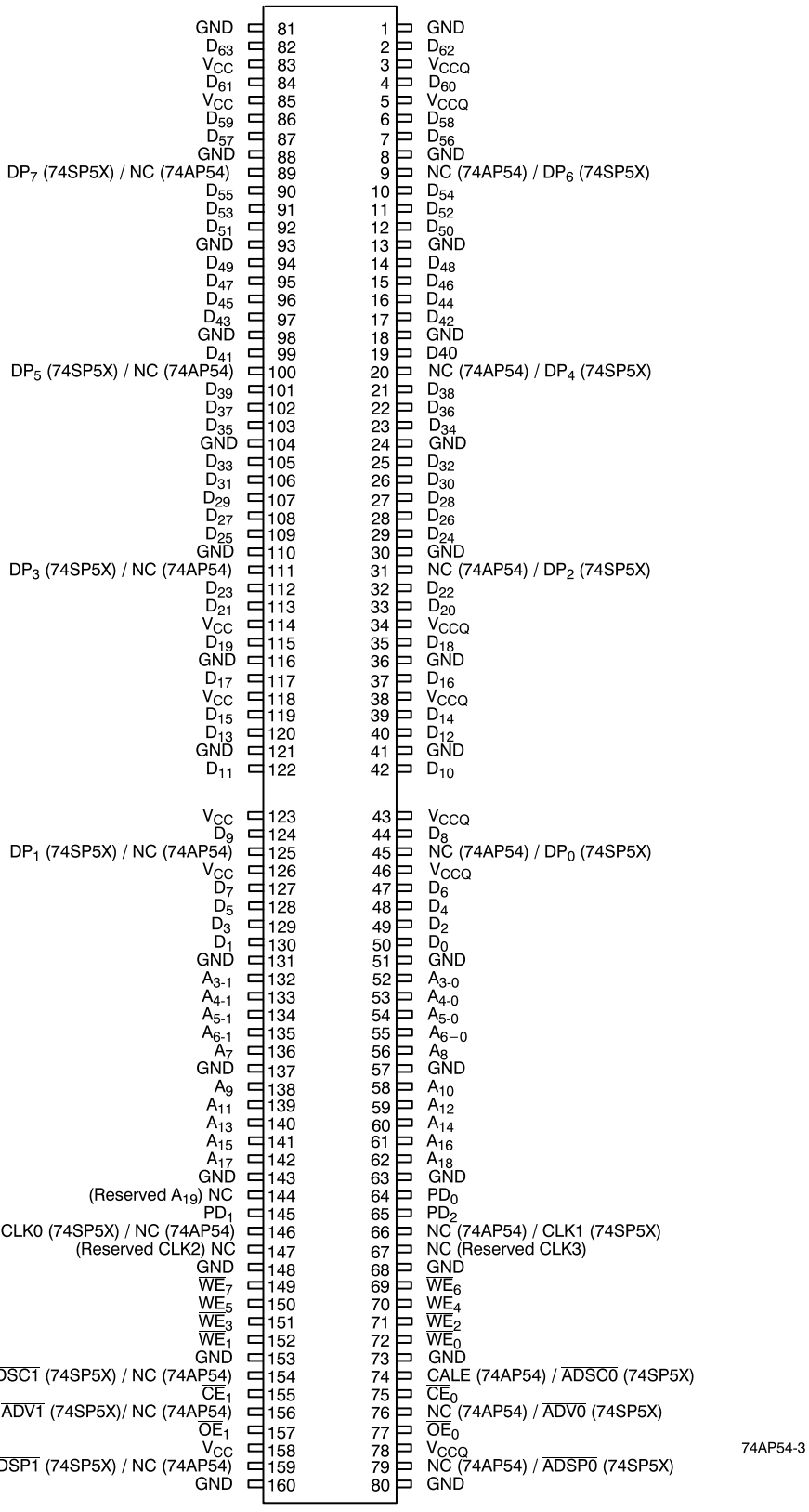


Selection Guide

	74AP54−60	74AP54−66	74SP54−60	74SP54−66	74SP55−60	74SP55−66
Cache Size (KB)	256	256	256	256	512	512
System Clock (MHz)	60	66	60	66	60	66
RAM Clock	Asynchronous	Asynchronous	Synchronous	Synchronous	Synchronous	Synchronous
RAM Speed	t_{AA}=15 ns	t_{AA}=12 ns	t_{CDV}=10.5 ns	t_{CDV}=8.5 ns	t_{CDV}=10.5 ns	t_{CDV}=8.5 ns

Pin Configuration

Dual Read-Out SIMM (DIMM)
Top View



74AP54-3

Pin Definitions

Signal Name	Description
V_{CC}	5V Supply
V_{CCQ}	3.3V Supply
GND	Ground
A_7-A_{19}	Addresses from processor
A_{3-0}, A_{4-0}, A_{5-0}, A_{6-0}	Lower address from chip set, identical to the bank1 addresses
A_{3-1}, A_{4-1}, A_{5-1}, A_{6-1}	Lower address from chip set, identical to the bank0 addresses
$\overline{CE}_0$, $\overline{CE}_1$	Chip Enable (same signal)
$\overline{OE}_0$, $\overline{OE}_1$	Output Enable (same signal)
$\overline{WE}_0$, $\overline{WE}_1$, $\overline{WE}_2$, $\overline{WE}_3$, $\overline{WE}_4$, $\overline{WE}_5$, $\overline{WE}_6$, $\overline{WE}_7$	Byte Write Enables
CALE	Latch Enable − CYM74AP54 only
PD_0-PD_2	Presence Detect pins
D_0-D_{63}	Data lines from processor
DP_0-DP_7	Data Parity lines (Optional), CYM74SP54 or CYM74SP55 only
$\overline{ADSP0}$, $\overline{ADSP1}$	Processor Address Strobe, CYM74SP54 or CYM74SP55 only
$\overline{ADSC0}$,$\overline{ADSC1}$	Cache Controller Address Strobe, CYM74SP54 or CYM74SP55 only
$\overline{ADV0}$, $\overline{ADV1}$	Burst Address Advance − CYM74SP54 or CYM74SP55 only
CLK0, CLK1, CLK2, CLK3	Clock signals − CYM74SP54 or CYM74SP55 only, should be given own clk drivers
NC	Signal not connected on module.

Presence Detect Pins

	PD_2	PD_1	PD_0
Asynchronous − CYM74AP54	NC	GND	NC
Synchronous − CYM74SP54	GND	GND	NC
Synchronous − CYM74SP55	GND	GND	GND

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −55°C to +125°C

Ambient Temperature with Power Applied ..... −0°C to +70°C

3.3V Supply Voltage to Ground Potential .... −0.5V to +4.6V

5V Supply Voltage to Ground Potential ..... −0.5V to +5.25V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +4.6V

DC Input Voltage ..... −0.5V to +4.6V

Output Current into Outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5% 3.3V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Condition	Min.	Max.	Unit
V_{IH}	Input HIGH Voltage		2.2	V_{CCQ} + 0.3	V
V_{IL}	Input LOW Voltage		−0.3	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC}=Min. I_{OH} = −4 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC}=Min. I_{OL} = 8 mA		0.4	V
I_{CC} (74AP54)	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		1500	mA
I_{CC} (74SP54)	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		1500	mA
I_{CC} (74SP55)	V_{CC} Operating Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=f_{MAX}=1/t_{RC}		1500	mA

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Description	Operating Range
60	CYM74AP54PM−60C	PM25	160-Pin Dual-Readout SIMM	Asynchronous, 15-ns Access RAMs	Commercial
	CYM74SP54PM−60C	PM26	160-Pin Dual-Readout SIMM	Synchronous	
	CYM74SP55PM−60C	PM26	160-Pin Dual-Readout SIMM	Synchronous	
66	CYM74AP54PM−66C	PM25	160-Pin Dual-Readout SIMM	Asynchronous, 12-ns Access RAMs	Commercial
	CYM74SP54PM−66C	PM26	160-Pin Dual-Readout SIMM	Synchronous	
	CYM74SP55PM−66C	PM26	160-Pin Dual-Readout SIMM	Synchronous	

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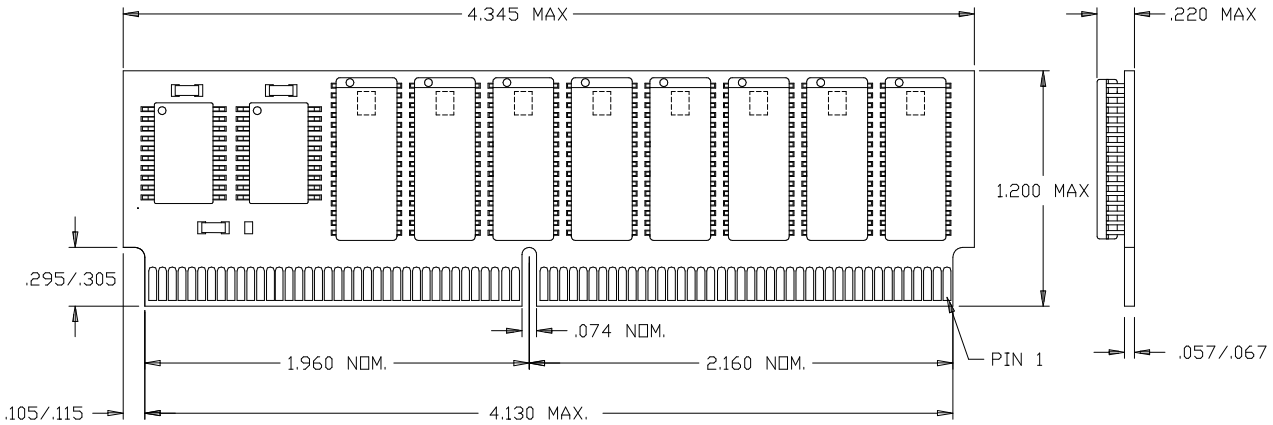
Package Diagrams

160-Pin Dual-Readout SIMM PM25



160-Pin Dual-Readout SIMM PM26