CYM9244, CYM9245 CYM9246, CYM9247

128K/256K Cache Module Family for the OPTi 802GP Chip Set

Features

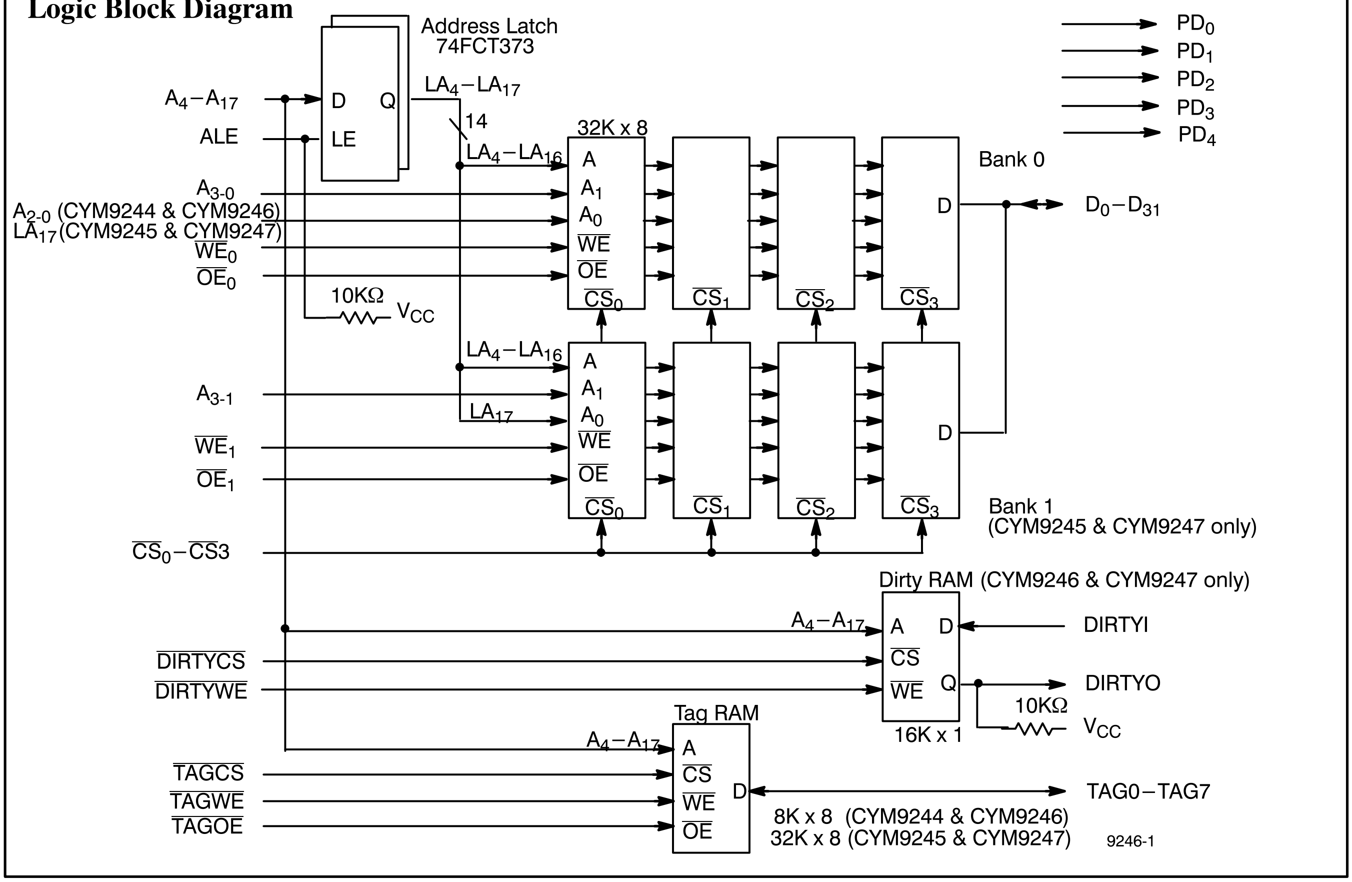
- **128 Kbyte (CYM9244 & CYM9246), 256 Kbyte (CYM9245 & CYM9247), secondary cache modules**
- **Ideal for Intel™ 486 systems with the OPTi 802GP chip-set**
- **Zero-wait-state operations at 33 MHz**
- **Constructed using cost-effective CMOS asynchronous SRAMs**
- **On-board decoupling capacitors offer improved noise immunity**
- **112-position Burndy connector, part # CELP2X56SC3Z48**
- **5V (±5%) power supply**
- **TTL-compatible inputs/outputs**

Functional Description

These modules are designed to function as the secondary cache in Intel 486-based systems with the OPTi 802GP chip-set. Each module contains either one or two banks of 32-bit wide data SRAMs, an 8-bit wide tag RAM, and a single-bit dirty RAM with separate I/O (CYM9246 and CYM9247 only). The addresses for the data SRAMs are buffered by an on-board latch. Asynchronous CMOS SRAMs are used to provide a low-cost, low-power, and zero-wait-state solution for CPU speeds up to 33 MHz. Multiple ground pins and on-board decoupling capacitors ensure maximum protection from noise.

Each module interfaces with the rest of the system via a 112-pin Burndy connector. All components on the cache module are surface mounted on a multi-layer epoxy laminate (FR-4) board. The package dimensions are 3.15″ x 0.365″ x 1.1″. All inputs and outputs of the CYM9244, CYM9245, CYM9246, and CYM9247 cache modules are TTL compatible and operate from a single 5V power supply. The contact pins are plated with 100 micro-inches of nickel covered by 10 micro-inches of gold flash.

Logic Block Diagram



Selection Guide

	CYM9244PB−20C	CYM9245PB−20C	CYM9246PB−20C	CYM9247PB−20C
Cache Size (KB)	128	256	128	256
Data SRAM (ns)	20	20	20	20
Dirty SRAM (ns)			20	20
Tag/Valid SRAM (ns)	15	15	15	15

Pin Configuration

Dual Read-out SIMM
Top View

GND	57	1	GND
D_0	58	2	D_1
D_2	59	3	D_3
D_4	60	4	D_5
D_6	61	5	D_7
V_{CC}	62	6	V_{CC}
NC	63	7	NC
D_8	64	8	D_9
D_{10}	65	9	D_{11}
D_{12}	66	10	D_{13}
GND	67	11	GND
D_{14}	68	12	D_{15}
D_{16}	69	13	D_{17}
D_{18}	70	14	D_{19}
D_{20}	71	15	D_{21}
V_{CC}	72	16	V_{CC}
D_{22}	73	17	D_{23}
NC	74	18	NC
D_{24}	75	19	D_{25}
D_{26}	76	20	D_{27}
GND	77	21	GND
D_{28}	78	22	D_{29}
D_{30}	79	23	D_{31}
(CYM9244 & CYM9246) A_{2-0}	80	24	A_{2-1} (not used)
A_{3-0}	81	25	A_{3-1} (CYM9245 & CYM9247)
V_{CC}	82	26	V_{CC}
A_4	83	27	A_5
A_6	84	28	A_7
A_8	85	29	A_9
A_{10}	86	30	A_{11}
A_{12}	87	31	A_{13}
A_{14}	88	32	A_{15}
A_{16}	89	33	A_{17}
A_{18}	90	34	NC
GND	91	35	GND
(CYM9246 & CYM9247) DIRTYI	92	36	DIRTYO (CYM9246 & CYM9247)
TAG0	93	37	TAG1
TAG2	94	38	TAG3
TAG4	95	39	TAG5
GND	96	40	GND
TAG6	97	41	TAG7
NC	98	42	NC
$\overline{TAGCS}$	99	43	ALE
$\overline{TAGWE}$	100	44	$\overline{CS}_0$
V_{CC}	101	45	V_{CC}
GND	102	46	GND
$\overline{TAGOE}$	103	47	$\overline{CS}_1$
(CYM9246 & CYM9247) $\overline{DIRTYWE}$	104	48	$\overline{CS}_2$
(CYM9246 & CYM9247) $\overline{DIRTYCS}$	105	49	$\overline{CS}_3$
V_{CC}	106	50	V_{CC}
$\overline{OE}_0$	107	51	$\overline{OE}_1$ (CYM9245 & CYM9247)
$\overline{WE}_0$	108	52	$\overline{WE}_1$ (CYM9245 & CYM9247)
PD_0	109	53	PD_1
PD_2	110	54	PD_3
PD_4	111	55	NC
GND	112	56	GND

9246-2

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −55°C to +125°C

Ambient Temperature with Power Applied .... −0°C to +70°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −0.5V to +7.0V

Output Current into Outputs (LOW) .... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%

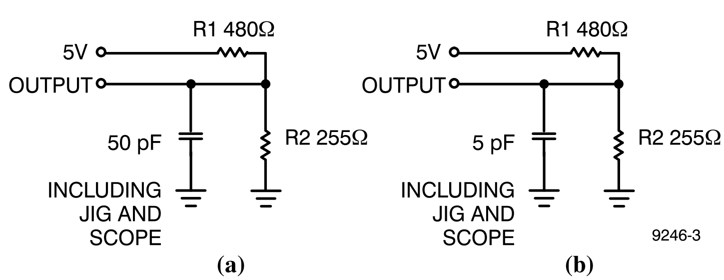
Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CYM9244, CYM9245, CYM9246, CYM9247		Unit
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}+0.3	V
V_{IL}	Input LOW Voltage		−0.5	0.8	V
I_{CC}	V_{CC} Operating Supply Current (CYM9244)	V_{CC}=Max., I_{OUT}=0 mA, $f=f_{MAX}=1/t_{RC}$		950	mA
I_{CC}	V_{CC} Operating Supply Current (CYM9245)	V_{CC}=Max., I_{OUT}=0 mA, $f=f_{MAX}=1/t_{RC}$		1700	mA
I_{CC}	V_{CC} Operating Supply Current (CYM9246)	V_{CC}=Max., I_{OUT}=0 mA, $f=f_{MAX}=1/t_{RC}$		1050	mA
I_{CC}	V_{CC} Operating Supply Current (CYM9247)	V_{CC}=Max., I_{OUT}=0 mA, $f=f_{MAX}=1/t_{RC}$		1800	mA

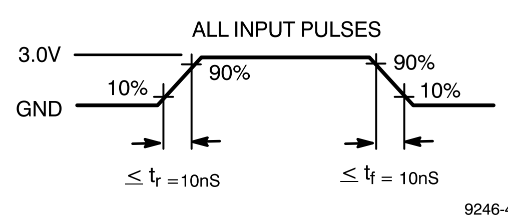
Presence Detect Table

	PD_4	PD_3	PD_2	PD_1	PD_0
CYM9244	NC	NC	NC	NC	GND
CYM9245	NC	NC	NC	GND	NC
CYM9246	GND	NC	NC	NC	GND
CYM9247	GND	NC	NC	GND	NC

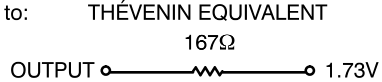
AC Test Loads and Waveforms



(a) (b)



Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics

Parameter	Description	Min.	Max.	Unit
ALE Timing				
t_{LE}	ALE HIGH to Change in Latched Address	8.5		ns
t_{PD}	Address Propagation Delay Through FCT373A Latch		5.2	ns
Data SRAM Read Timing				
t_{RC}	Read Cycle Time[1]	27		ns
t_{AA1}	Address Access Time (A_4-A_{17}, Latch Transparent)		27	ns
t_{AA2}	Address Access Time ($A_{2\text{-}0}$, $A_{3\text{-}0}$, $A_{3\text{-}1}$, No Latch Path)		22	ns
t_{OHA}	Output Hold from Address Change[2]	3		ns
t_{OE}	$\overline{\text{OE}}$[1:0] LOW to Output Valid		11	ns
t_{CE}	$\overline{\text{CS}}$[7:0] LOW to Data Output Valid		22	ns
t_{LZOE}	$\overline{\text{OE}}$[1:0] LOW to Low Z[2]	0		ns
t_{HZOE}	$\overline{\text{OE}}$[1:0] HIGH to High Z[2]		11	ns
t_{LZCE}	$\overline{\text{CS}}$[7:0] LOW to Low Z[2]	3		ns
t_{HZCE}	$\overline{\text{CS}}$[7:0] HIGH to High Z[2]		11	ns
t_{PU}	$\overline{\text{CS}}$[7:0] LOW to Power-Up[2]	0		ns
t_{PD}	$\overline{\text{CS}}$[7:0] HIGH to Power-Down[2]		22	ns
Tag SRAM Read Timing				
t_{TRC}	Tag Read Cycle Time[1]	17		ns
t_{TTAA}	Tag Address Access Time		17	ns
t_{TOHA}	Tag Output Hold from Address Change[2]	3		ns
t_{TCS}	$\overline{\text{TAGCS}}$ LOW to Tag Valid		17	ns
t_{TOE}	$\overline{\text{TAGOE}}$ LOW to Tag Valid		9	ns
t_{TLZOE}	$\overline{\text{TAGOE}}$ LOW to Tag Low Z[2]	0		ns
t_{THZOE}	$\overline{\text{TAGOE}}$ HIGH to Tag High Z[2]		10	ns
t_{TLZCE}	$\overline{\text{TAGCS}}$ LOW to Tag Low Z[2]	3		ns
t_{THZCE}	$\overline{\text{TAGCS}}$ HIGH to Tag High Z[2]		10	ns
t_{TPU}	$\overline{\text{TAGCS}}$ LOW to Tag RAM Power-Up[2]	0		ns
Dirty SRAM Read Timing (CYM9246 & CYM 9247)				
t_{DRC}	Dirty Read Cycle Time[1]	22		ns
t_{DAA}	Dirty Address Access Time		22	ns
t_{DOHA}	DIRTYO Hold from Address Change[2]	1		ns
t_{DCS}	$\overline{\text{DIRTYCS}}$ LOW to DIRTYO Valid		20	ns
t_{DLZCE}	$\overline{\text{DIRTYCS}}$ LOW to DIRTYO Low Z[2]	5		ns
t_{DHZCE}	$\overline{\text{DIRTYCS}}$ HIGH to DIRTYO High Z[2]		10	ns
t_{DPU}	$\overline{\text{DIRTYCS}}$ LOW to Dirty RAM Power-Up[2]	0		ns
t_{DPD}	$\overline{\text{DIRTYCS}}$ HIGH to Dirty RAM Power-Down[2]		17	ns

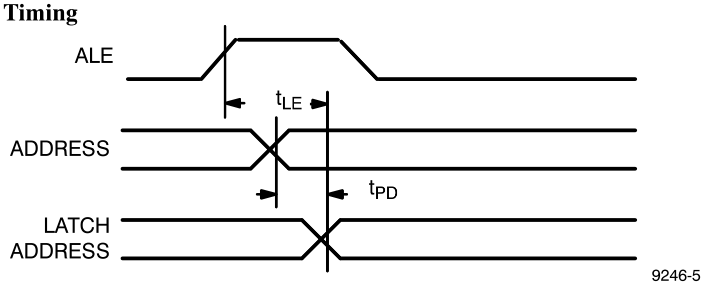
Switching Characteristics (continued)

Parameters	Description	Min.	Max.	Units
Data SRAM Write Timing				
t_{WC}	Write Cycle Time[1]	27		ns
t_{SCE}	$\overline{CS}$[7:0] LOW to End of Write[1]		22	ns
t_{AW1}	Address Set-Up to End of Write ($A_4 - A_{17}$)[1]	20		ns
t_{AW2}	Address Set-Up to End of Write ($A_{2\text{-}0}$, $A_{3\text{-}0}$, $A_{3\text{-}1}$, No Latch Path)[1]	15		ns
t_{HA}	Address Hold from End of Write [2]	0		ns
t_{SA}	Address Set-Up to Start of Write [2]	0		ns
t_{PWE}	$\overline{WE}$[1:0] Pulse Width[1]	15		ns
t_{SD}	Data Set-Up to End of Write[2]	12		ns
t_{HD}	Data Hold from End of Write[2]	0		ns
t_{LZWE}	$\overline{WE}$[1:0] LOW to High Z[2]		12	ns
t_{HZWE}	$\overline{WE}$[1:0] HIGH to Low Z[2]	3		ns
Tag SRAM Write Timing				
t_{TWC}	Tag Write Cycle Time[1]	17		ns
t_{TSCE}	$\overline{TAGCS}$ LOW to End of Tag Write[1]	10		ns
t_{TAW}	Address Set-Up to End of Tag Write [1]	10		ns
t_{THA}	Address Hold from End of Tag Write [2]	0		ns
t_{TSA}	Address Set-Up to Start of Tag Write [2]	0		ns
t_{TWPE}	$\overline{TAGWE}$ Pulse Width[1]	10		ns
t_{TSD}	Tag Set-Up to End of Tag Write[2]	11		ns
t_{THD}	Tag Hold from End of Tag Write[2]	0		ns
t_{TLZWE}	$\overline{TAGWE}$ LOW to Tag High Z[2]		9	ns
t_{THZWE}	$\overline{TAGWE}$ HIGH to Tag Low Z[2]	3		ns
Dirty SRAM Write Timing (CYM9246 & CYM9247)				
t_{DWC}	Dirty Write Cycle Time[1]	27		ns
t_{DDW}	DIRTYI Set-Up to End of Dirty Write [1]	12		ns
t_{DDHW}	DIRTYI Hold from End of Dirty Write [1]	0		ns
t_{DSCE}	$\overline{DIRTYCS}$ LOW to End of Dirty Write[2]	12		ns
t_{DAW}	Address Set-Up to End of Dirty Write [2]	16		ns
t_{DHA}	Address Hold from End of Dirty Write [2]	0		ns
t_{DSA}	Address Set-Up to Start of Dirty Write [2]	0		ns
t_{DWPE}	$\overline{DIRTYWE}$ Pulse Width[1]	12		ns
t_{DLZWE}	$\overline{DIRTYWE}$ LOW to DIRTYO pulled HIGH[2]		9	ns
t_{DHZWE}	$\overline{DIRTYWE}$ HIGH to DIRTYO Low Z[2]	5		ns

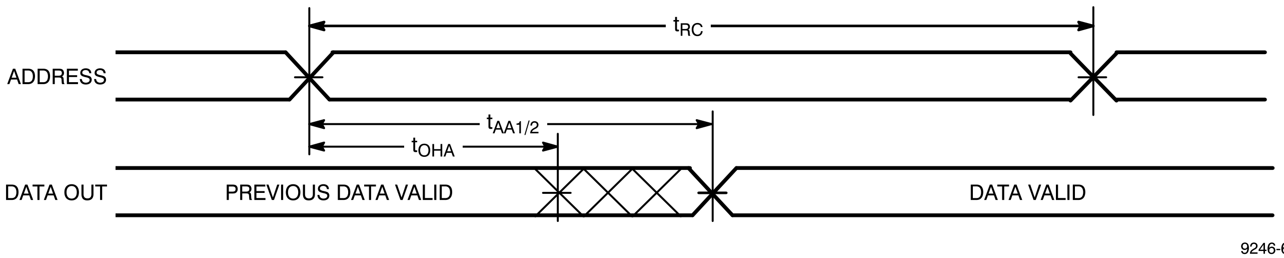
Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Parameters guaranteed by design, not tested.

Switching Waveforms

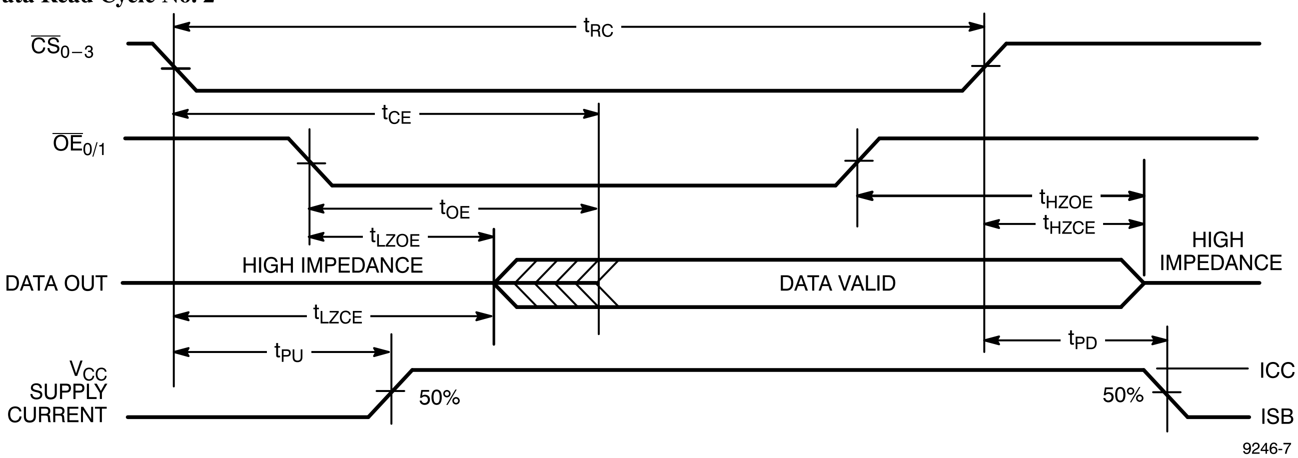
ALE Timing



Data Read Cycle No. 1[3, 4]



Data Read Cycle No. 2[14, 5]

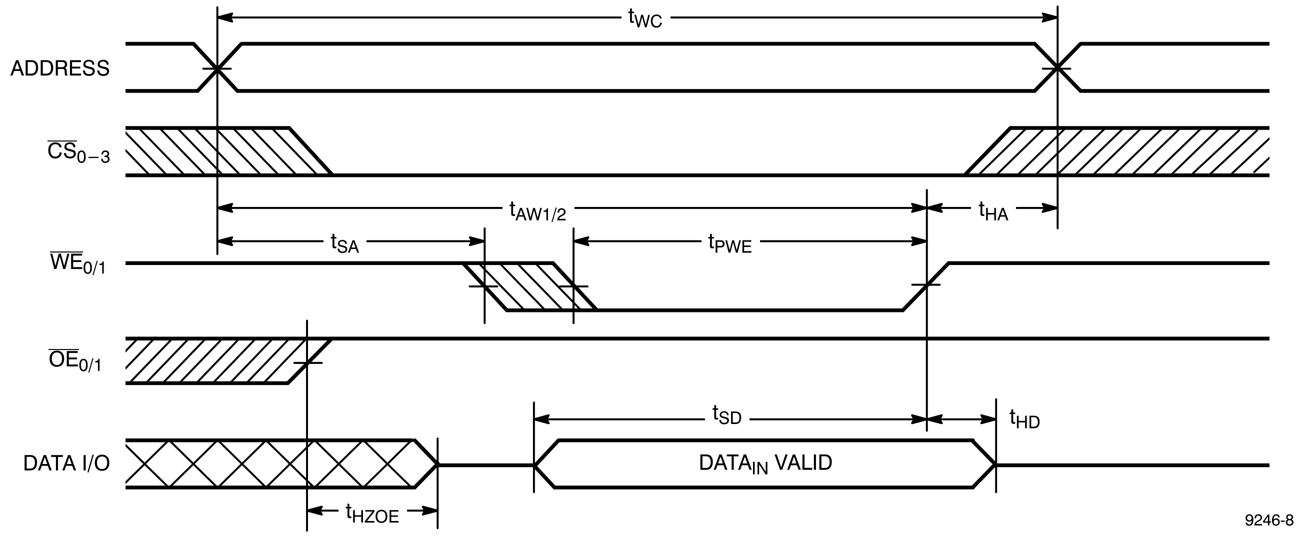


Notes:

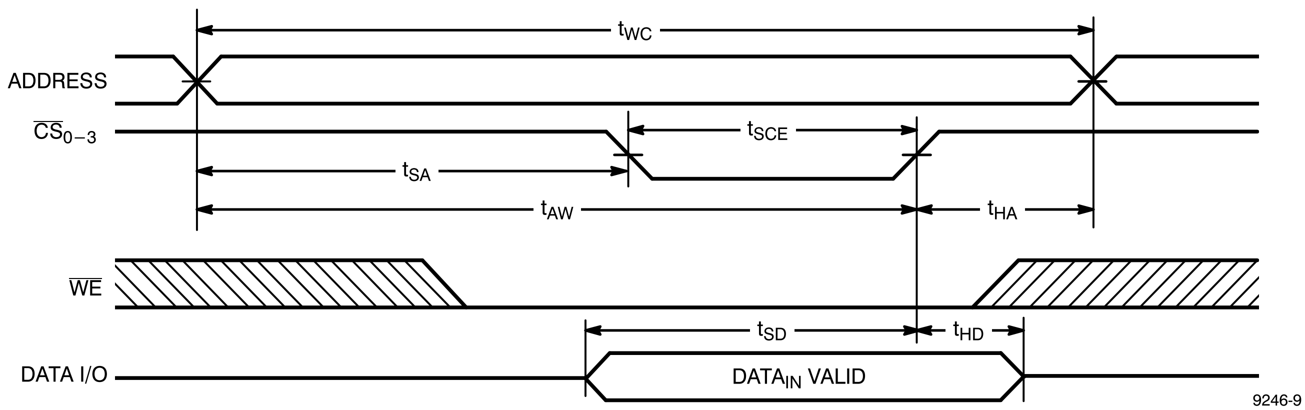
3. Device is continuously selected. $\overline{OE}_{0/1}$, $\overline{CS}_{0-3} = V_{IL}$.
4. $\overline{WE}_{0/1}$ is HIGH for read cycle.
5. Address valid prior to or coincident with $\overline{CS}_0 - \overline{CS}_3$ transition LOW.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms (continued)

Data Write Cycle No. 1 ($\overline{WE}$ Controlled)[6, 7, 8]



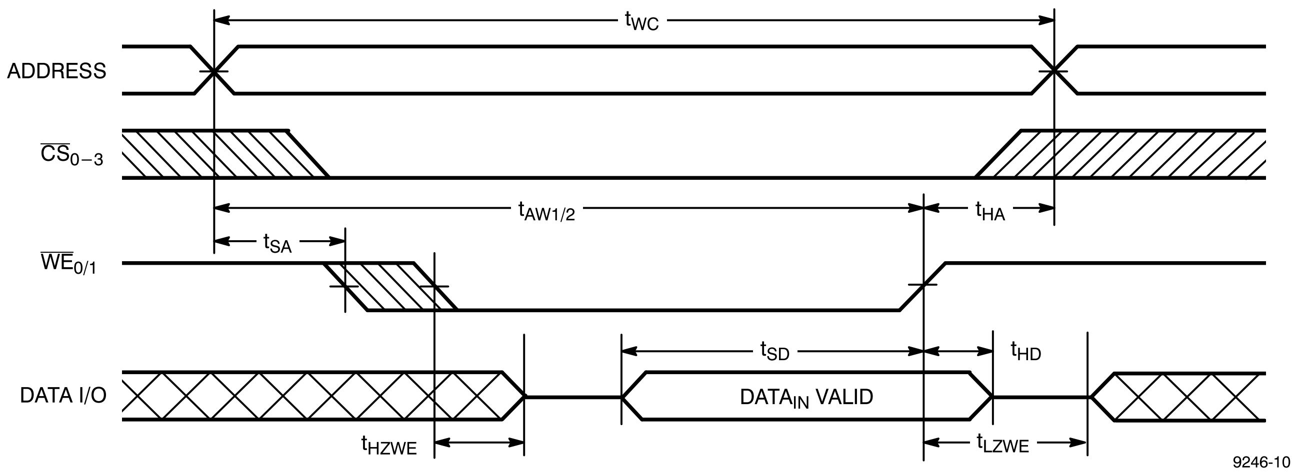
Data Write Cycle No. 2 ($\overline{CS}$[0−3] Controlled)[16, 17, 8]



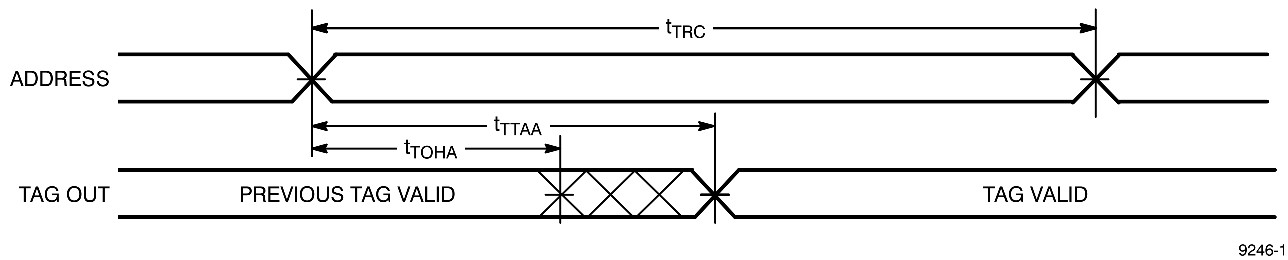
Notes:

7. Data I/O is high impedance if $\overline{OEO}/1 = V_{IH}$.
8. If $\overline{CS}_0 - \overline{CS}_3$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Data Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[8, 9]



Tag Read Cycle No. 1[10, 11]

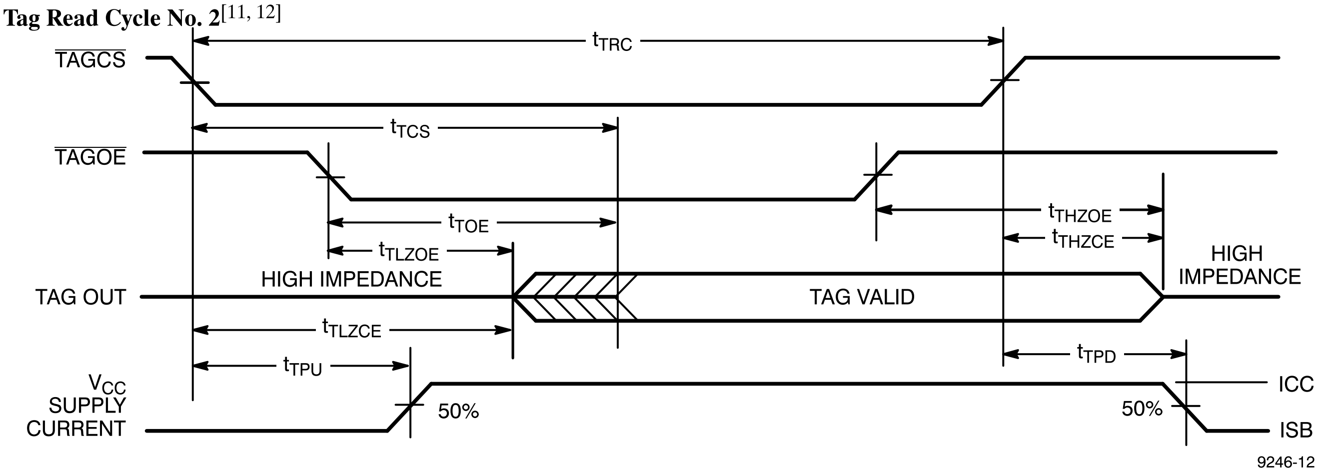


Notes:

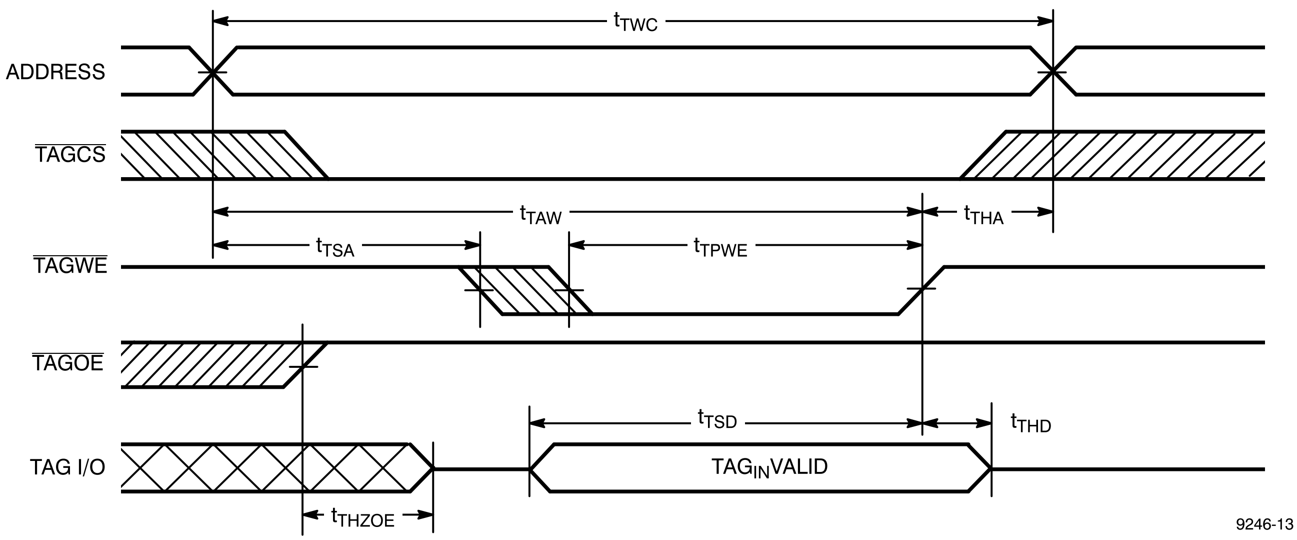
9. The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.
10. Device is continuously selected. $\overline{TAGOE}$, $\overline{TAGCS}$ = V_{IL}.
11. $\overline{TAGWE}$ is HIGH for read cycle.

Switching Waveforms (continued)

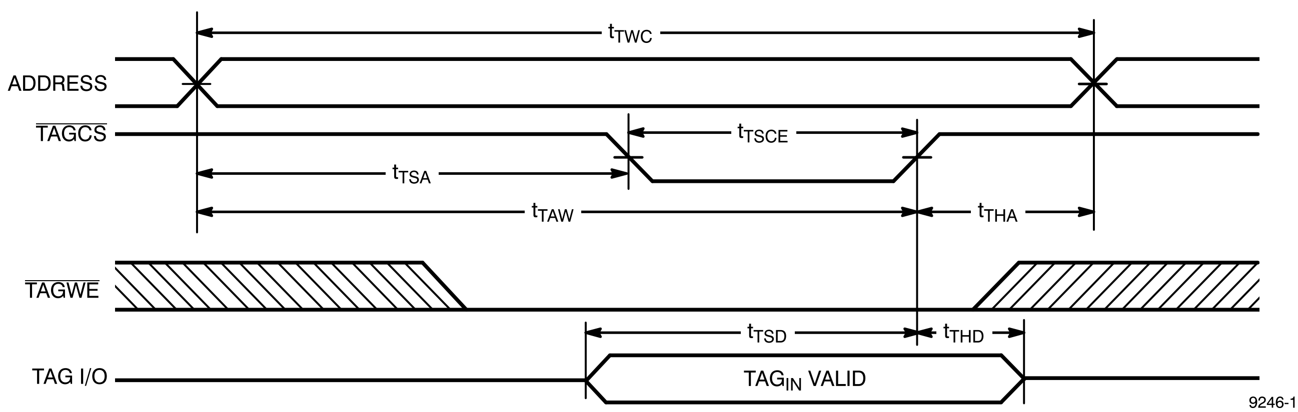
Tag Read Cycle No. 2[11, 12]



Tag Write Cycle No. 1 ($\overline{\text{TAGWE}}$ Controlled)[13, 14, 15]



Tag Write Cycle No. 2 ($\overline{\text{TAGCS}}$ Controlled)[13, 14, 15]

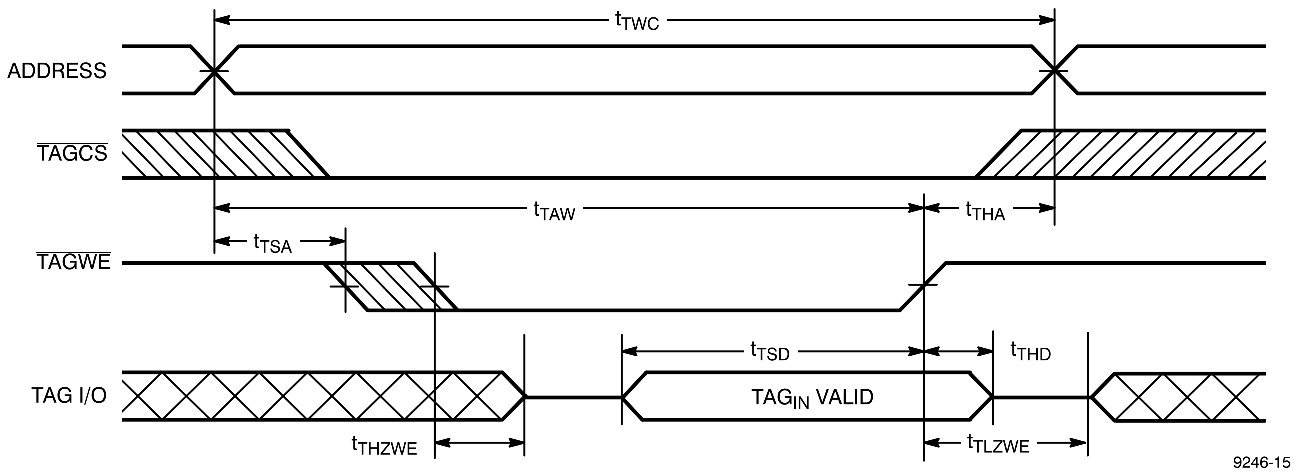


Notes:

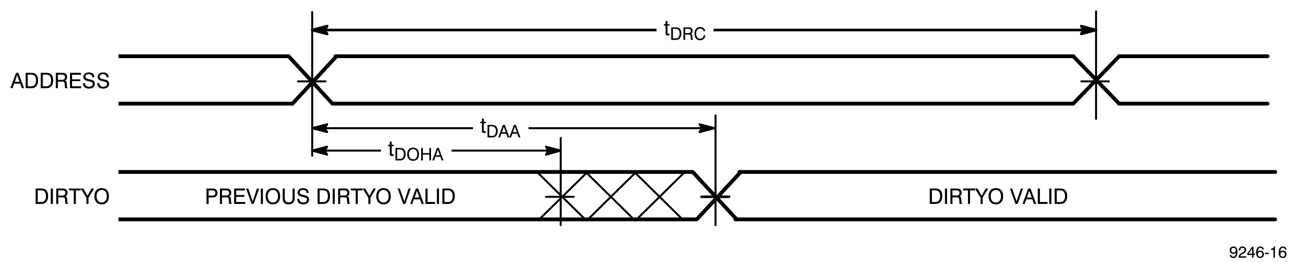
12. Address valid prior to, or coincident with $\overline{\text{TAGCS}}$ transition LOW.
13. The internal write time of the memory is defined by the overlap of $\overline{\text{TAGCS}}$ LOW and $\overline{\text{TAGWE}}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
14. TAG I/O is high impedance if $\overline{\text{TAGOE}}$ = LOW.

Switching Waveforms (continued)

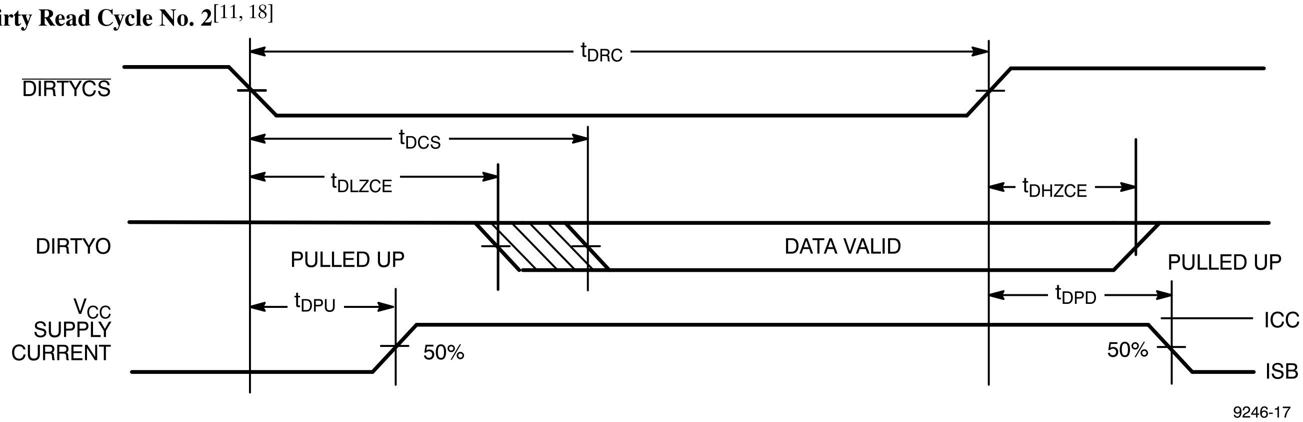
Tag Write Cycle No. 3 ($\overline{TAGWE}$ Controlled, $\overline{TAGOE}$ LOW)[15]



Dirty Read Cycle No. 1[16, 17]



Dirty Read Cycle No. 2[11, 18]

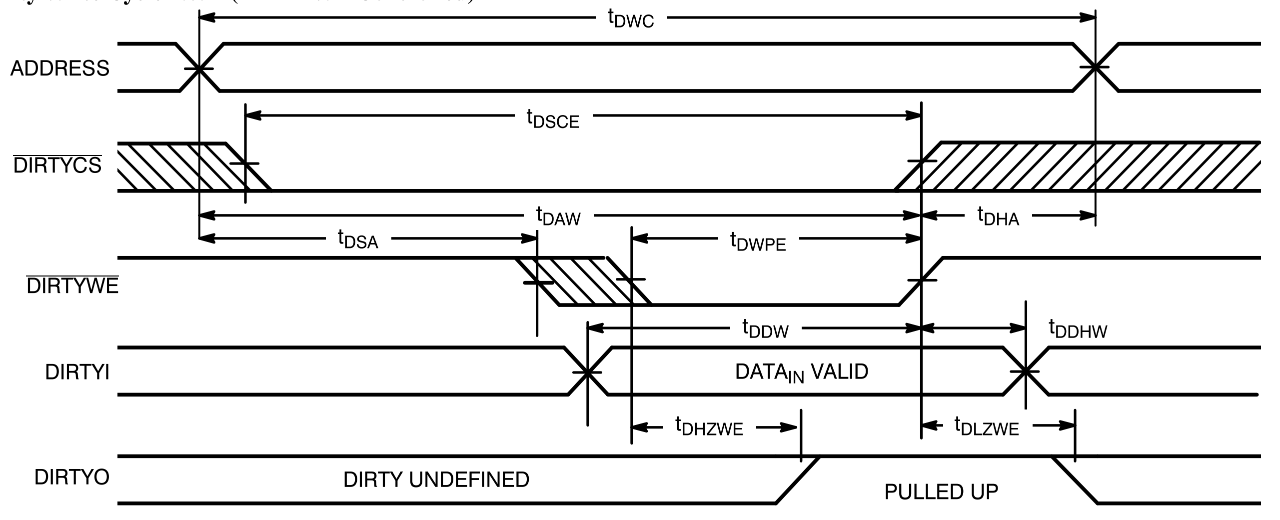


Notes:

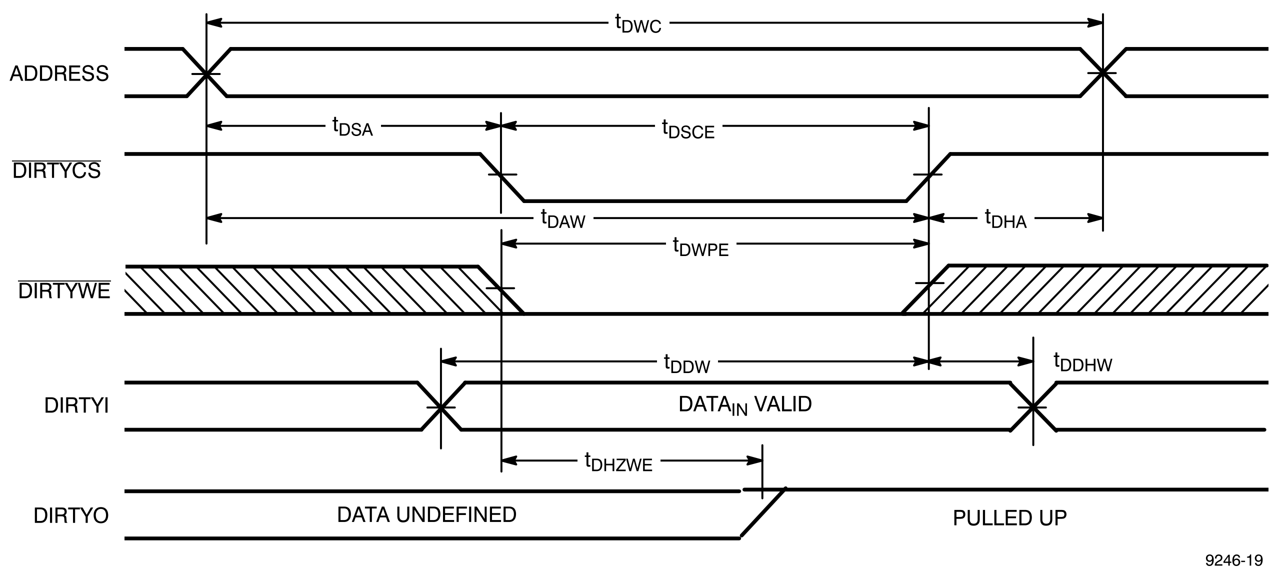
15. If $\overline{TAGCE}$ goes HIGH simultaneously with $\overline{TAGWE}$ HIGH, the output remains in a high-impedance state.
16. $\overline{DIRTYWE}$ is high for read cycle.
17. Device is continuously selected, $\overline{DIRTYCS} = V_{IL}$.
18. Address valid prior to or coincident with $\overline{DIRTYCS}$ transition LOW.

Switching Waveforms (continued)

Dirty Write Cycle No. 1 (DIRTYWE Controlled)[19]



Dirty Write Cycle No. 2 (DIRTYCS Controlled)[19, 20]



Notes:

19. The internal write time of the memory is defined by the overlap of DIRTYCS LOW and DIRTYWE LOW. Both signals msut be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
20. If DIRTYCS goes HIGH simultaneously with DIRTYWE HIGH, the output remains in a high-impedance state.

Ordering Information

Cache Memory Size	Ordering Code	Package Name	Package Type	Operating Range
128 Kbyte	CYM9244PB−20C	PB17	112-Pin Dual-Readout SIMM	Commercial
256 Kbyte	CYM9245PB−20C	PB18	112-Pin Dual-Readout SIMM	Commercial
128 Kbyte	CYM9246PB−20C	PB17	112-Pin Dual-Readout SIMM	Commercial
256 Kbyte	CYM9247PB−20C	PB18	112-Pin Dual-Readout SIMM	Commercial

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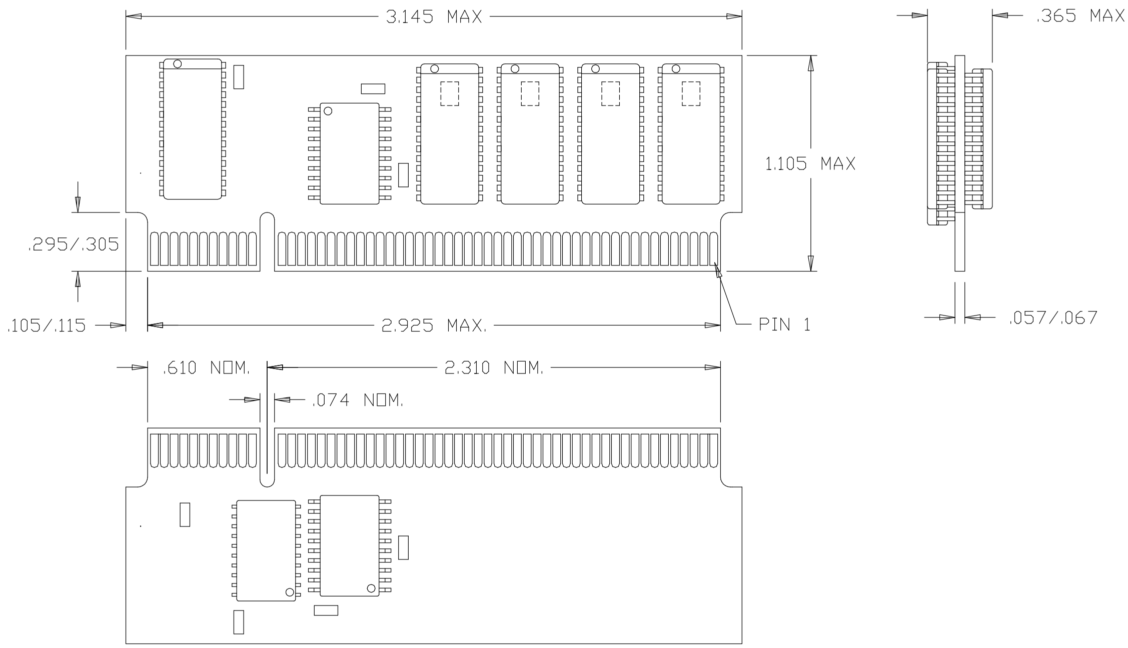
Package Diagrams

112-Pin Dual-Readout SIMM PB17



112-Pin Dual-Readout SIMM PB18