CY27C64

8K x 8 EPROM

Features

- **CMOS for optimum speed/power**
- **Windowed for reprogrammability**
- **High speed**
  - **— 70 ns (commercial)**
- **Low power**
  - **— 440 mW (commercial)**
  - **— 530 mW (military)**
- **Super low standby power**
  - **— Less than 85 mW when deselected**
- **EPROM technology 100% programmable**
- **5V ±10% V_{CC}, commercial and military**
- **TTL-compatible I/O**

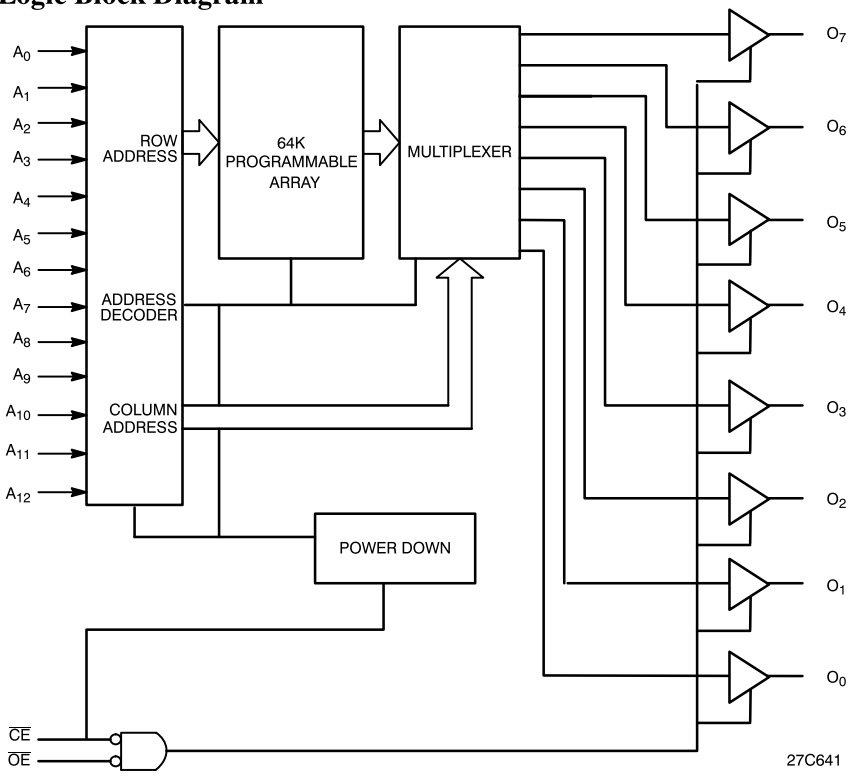
Functional Description

The CY27C64 is a high-performance 8192 word by 8 bit CMOS PROM. When deselected, the CY27C64 automatically powers down into a low-power standby mode. It is packaged in a 600-mil-wide package. The reprogrammable packages are equipped with an erasure window; when exposed to UV light, these EPROMs are erased and can then be reprogrammed. The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms.

The EPROM cell requires only 12.5V for the super voltage and low-current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each EPROM is also tested for AC performance to guarantee that after customer programming, the product will meet DC and AC specification limits.

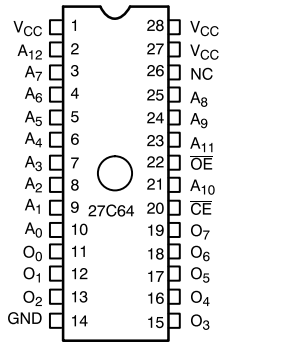
Reading is accomplished by placing an active LOW signal on $\overline{OE}$ and $\overline{CE}$. The contents of the memory location addressed by the address lines (A_0 through A_{12}) will become available on the output lines (O_0 through O_7).

Logic Block Diagram



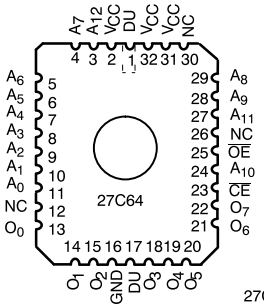
Pin Configurations

DIP/CerDIP
Top View



27C6423

PLCC[1]
Top View



27C6434

Selection Guide

		27C64−70	27C64−90	27C64−120	27C64−150	27C64−200
Maximum Access Time (ns)		70	90	120	150	200
Maximum Operating Current (mA)	Commercial	80	80	80	80	80
	Military	100	100	100	100	100
Maximum Standby Current (mA)	Commercial	15	15	15	15	15
	Military	15	15	15	15	15

Note:
1. Pins 1 and 17 are common and tied to the die attach pad. They should not be used.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (DIP Pin 28 to Pin 14) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage 13.0V

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... > 200 mA

UV Exposure ..... 7258 Wsec/cm^2

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[2]	−40°C to +85°C	5V ± 10%
Military[3]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[4, 5]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0		V
V_{IL}	Input LOW Voltage				0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	μA
V_{CD}	Input Diode Clamp Voltage			Note 5		
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		−10	+10	μA
I_{OS}	Output Short Circuit Current[6]	V_{CC} = Max., V_{OUT} = GND		−20	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = 2.0V, I_{OUT} = 0 mA f=10 MHz	Com'l		80	mA
			Mil		100	
I_{SB}	Standby Supply Current	Chip Enable Inactive, $\overline{CE}$ = V_{IH}, I_{OUT} = 0 mA	Com'l		15	mA
			Mil		15	

Capacitance[5]

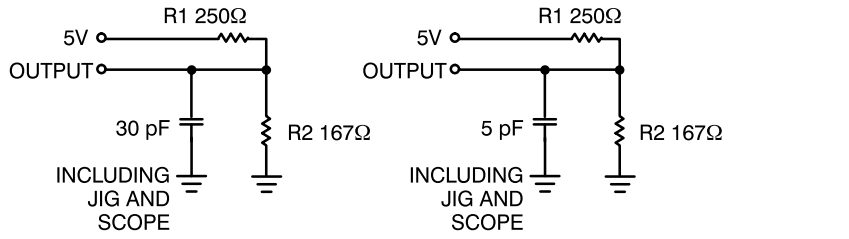
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

2. Contact a Cypress representative regarding industrial temperature range specification.
3. T_A is the "instant on" case temperature.
4. See the last page of this specification for Group A subgroup testing information.
5. See the "Introduction to CMOS NVMs" section of the Cypress Data Book for general information on testing.
6. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

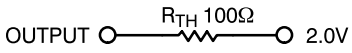
AC Test Loads and Waveforms

Test Load



(a) Normal Load **(b) High Z Load** 27C6445

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[2, 3, 5]

Parameter	Description	27C64−70		27C64−90		27C64−120		27C64−150		27C64−200		Unit
		Min.	Max	Min.	Max	Min.	Max	Min.	Max	Min.	Max	
t_{AA}	Address to Output Valid		70		90		120		150		200	ns
t_{HZCE}	Chip Enable Inactive to High Z		45		45		45		45		45	ns
t_{HZOE}	Output Enable Inactive to High Z		25		25		30		30		30	ns
t_{OE}	Output Enable Active to Output Valid		40		40		50		50		50	ns
t_{CE}	Chip Enable Active to Output Valid		70		90		120		150		200	ns
t_{OH}	Data Hold from Address Change	3		3		3		3		3		ns
t_{PU}	Chip Enable Active to Power-Up		70		90		120		150		200	ns
t_{PD}	Chip Enable Inactive to Power-Down		70		90		120		150		200	ns

Erasure Characteristics

Wavelengths of light less than 4000 angstroms begin to erase the devices in the windowed package. For this reason, an opaque label should be placed over the window if the EPROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The CY27C64 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the EPROM is exposed to high-intensity UV light for an extended period of time.

7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative. When programming, select the Cypress CY7C266 algorithm.

Table 1. Mode Selection

Mode		Pin Function[7, 8]							
	Normal Operation	**A_8**	**A_9**	**A_{10}**	**A_{11}**	**A_{12}**	**$\overline{CE}$**	**$\overline{OE}$**	**$D_7 - D_0$**
	Program	**$\overline{VFY}$**	**$\overline{PGM}$**	**LAT**	**NA**	**NA**	**$\overline{CE}$**	**V_{PP}**	**$D_7 - D_0$**
Read		A_8	A_9	A_{10}	A_{11}	A_{12}	V_{IL}	V_{IL}	$O_7 - O_0$
Standby		X	X	X	X	X	V_{IH}	X	Three-Stated
Output Disable		A_8	A_9	A_{10}	A_{11}	A_{12}	V_{IL}	V_{IH}	Three-Stated
Program		V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{PP}	$D_7 - D_0$
Program Verify		V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{PP}	$O_7 - O_0$
Program Inhibit		V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{PP}	Three-Stated
Blank Check		V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{PP}	$O_7 - O_0$

Notes:
7. X = "don't care" but must not exceed V_{CC} + 5%.
8. Address $A_8 - A_{12}$ must be latched through lines $A_0 - A_4$ in Programming modes.

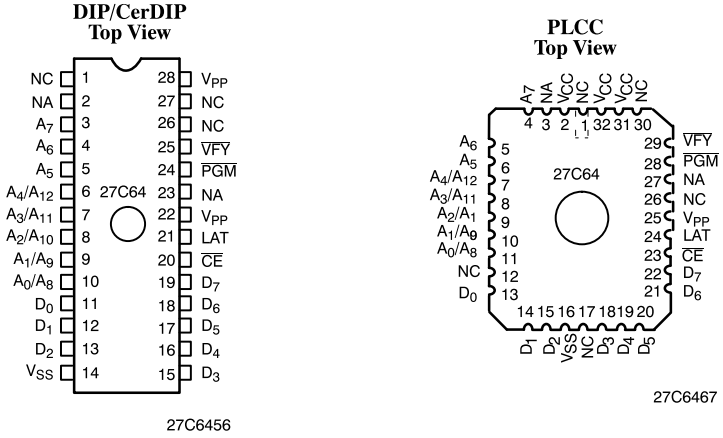
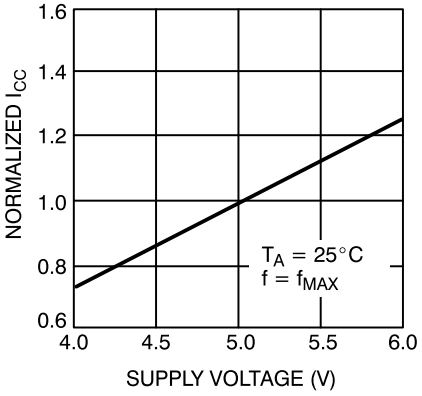


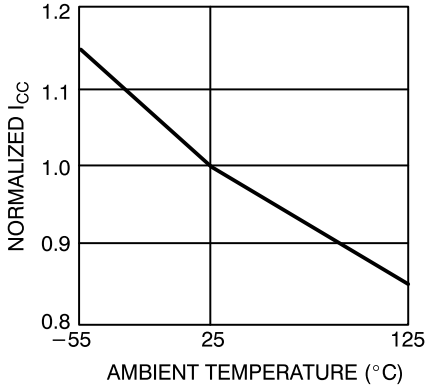
Figure 1. Programming Pinout

Typical DC and AC Characteristics

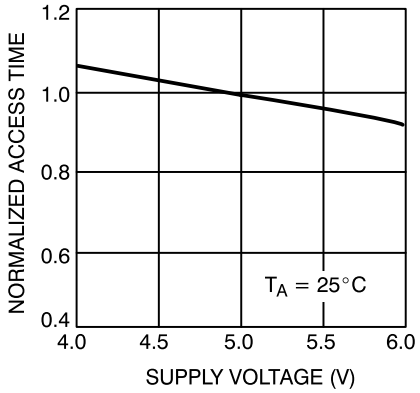
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



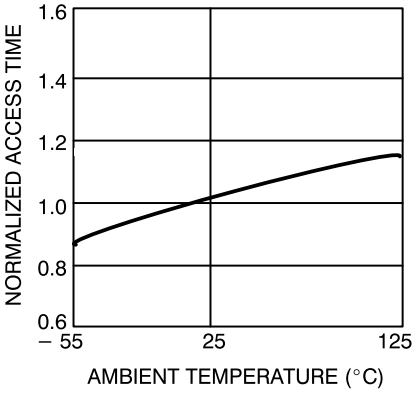
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



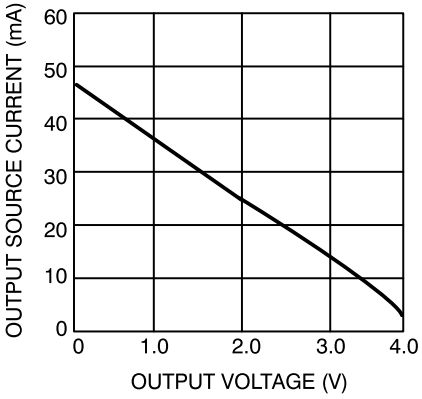
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



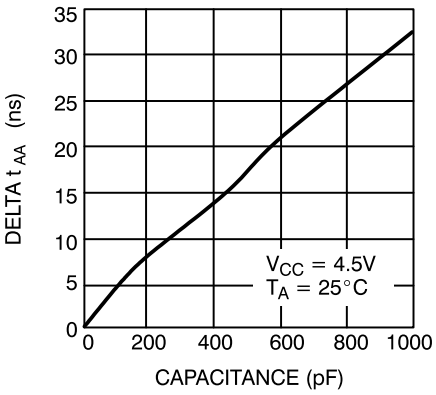
NORMALIZED ACCESS TIME vs. TEMPERATURE



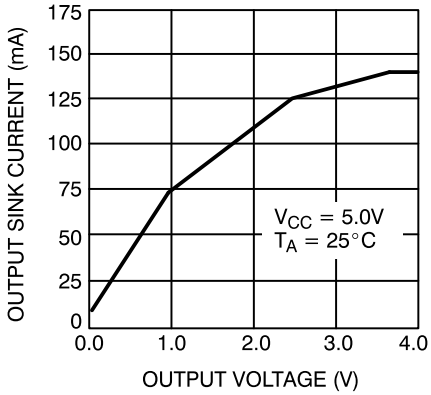
OUTPUT SOURCE CURRENT vs. VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



Ordering Information[9]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY27C64−70JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C64−70PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C64−70WC	W16	28-Lead (600-Mil) Windowed CerDIP	
90	CY27C64−90JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C64−90PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C64−90WC	W16	28-Lead (600-Mil) Windowed CerDIP	
120	CY27C64−120JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C64−120PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C64−120WC	W16	28-Lead (600-Mil) Windowed CerDIP	
150	CY27C64−150JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C64−150PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C64−150WC	W16	28-Lead (600-Mil) Windowed CerDIP	
200	CY27C64−200JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY27C64−200PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27C64−200WC	W16	28-Lead (600-Mil) Windowed CerDIP	

Note:

9. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

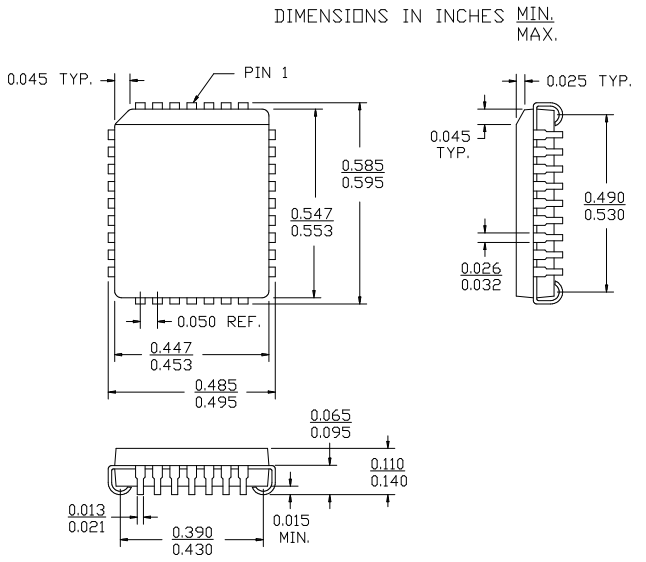
Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{OE}	7, 8, 9, 10, 11
t_{CE}	7, 8, 9, 10, 11

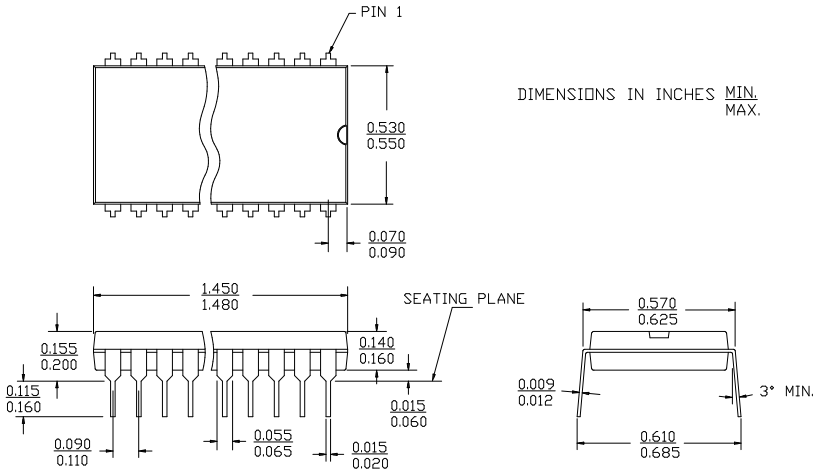
Document #: 38−00448

Package Diagrams

32-Lead Plastic Leaded Chip Carrier J65



28-Lead (600-Mil) Molded DIP P15



Package Diagrams (continued)

28-Lead (600-Mil) Windowed CerDIP W16
MIL−STD−1835 D−10 Config. A