Interfacing a 5V Cypress PROM to a 3.3V System using a CYBUS3384 Bus Switch

This application note describes a method for interfacing a high-speed 5V Cypress PROM to a 3.3V system. The I/O level translation is achieved using a CYBUS3384 Bus Switch.

PROMs (Programmable Read Only Memories) are often used for code storage and can interface directly to the host processor bus. Many applications use fast Cypress PROMs to read code directly from the PROM (instead of downloading the code to a fast SRAM that administers the code to the processor). If a 3.3V host processor is being used that is not "5V safe," input levels may be exceeded and problems can arise. Additionally, high speed 3.3V PROMs may be difficult to locate. Using slower 3.3V PROMs can either decrease system performance or increase system cost, or both. Fortunately, this dilemma can be resolved by using a CYBUS3384 Bus switch to translate from 5V to 3.3V compatible levels with essentially no timing penalty. Since there is no speed penalty, the same high-speed 5V Cypress PROM can be used to achieve the same performance level. This immediate translation is essential to preserving system timing in high speed systems.

The CYBUS3384 was originally designed to three-state signals for busing applications. Due to the symetric nature of the MOS device being used, the CYBUS3384 can also be used in bidirectional applications (e.g., I/O pins commonly used on SRAMs). The "switch" consists of a simple NMOS pass gate controlled by a common (active LOW) enable signal as shown in *Figure 1*. When a LOW signal is applied to the control line, the signal applied to one side of the switch (side A) is allowed to propagate directly through to the output on the other side (side B). A HIGH signal applied to the control line would prevent the input from propagating to the output and would place the output in a high impedance, three-state condition. The output of the pass gate is a function of both the gate and drain voltages. The gate voltage is a function of V_{CC}. Therefore, by regulating V_{CC} of the Bus Switch we are able to control the voltage applied to the gate of the pass gate,

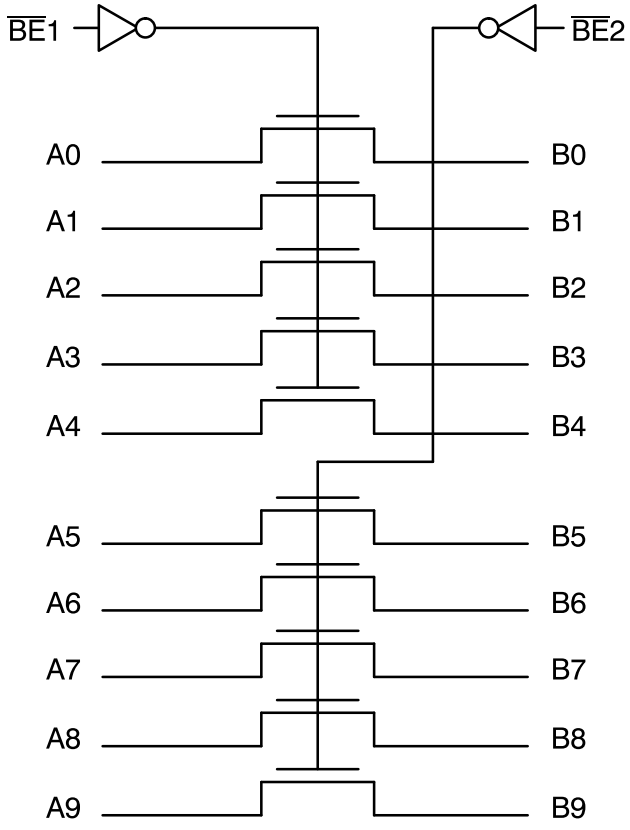

Figure 1. Configuration of the Bus Switch

which in turn limits the output swing of the device. If V_{CC} is properly regulated, the output levels can be 3.3V compatible.

The critical requirement for this circuit is to limit the V_{CC} applied to the Bus Switch. This can easily be accomplished with the existing 5V power supply and a simple zener diode-resistor network as shown in *Figure 2*. By adjusting either the resistor value or changing the zener diode, the V_{CC} applied to the Bus Switch and the output levels can be tuned to the desired values. For a 5V−>3.3V conversion, the resistor used should be between 40−100 ohms (1/4 watt) and the zener diode has a Vz=4.3V (I_{ZT}=10 mA). A 3.9V Zener can be used if a smaller I/O swing is desired. This type of configuration will only draw approximately 10 mA. It is important to select a low-current zener diode so the desired results can be achieved without burning excess power.

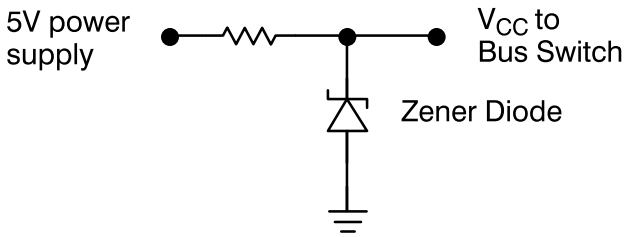

Figure 2. Regulator Circuit

The best feature of this 5V/3.3V translation is that no speed penalty is incurred. The maximum delay through the CYBUS3384 is 250 ps, well below the guardband of most high-speed designs. Therefore, Cypress's high-speed 5V PROMs can be used in 3.3V systems without any speed penalty by merely translating the I/O levels.

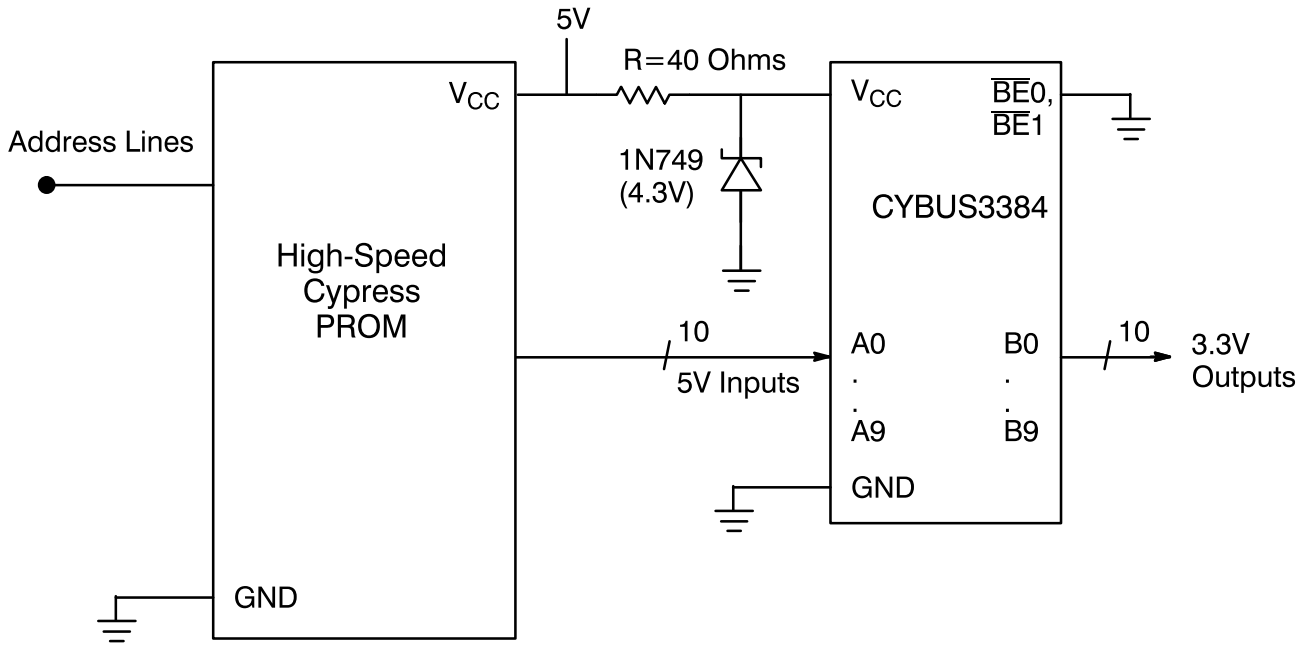

Figure 3. Final Implementation