CY7C287

64K x 8 Reprogrammable Registered PROM

Features

- **CMOS for optimum speed/power**
- **Windowed for reprogrammability**
- **High speed**
  - **— t_{SA} = 45 ns**
  - **— t_{CO} = 15 ns**
- **Low power**
  - **— 120 mA**
- **On-chip, edge-triggered output registers**
- **Programmable synchronous or asynchronous output enable**
- **EPROM technology, 100% programmable**
- **5V ±10% V_{CC}, commercial and military**
- **TTL-compatible I/O**
- **Slim 300-mil package**
- **Capable of withstanding >2001V static discharge**

Functional Description

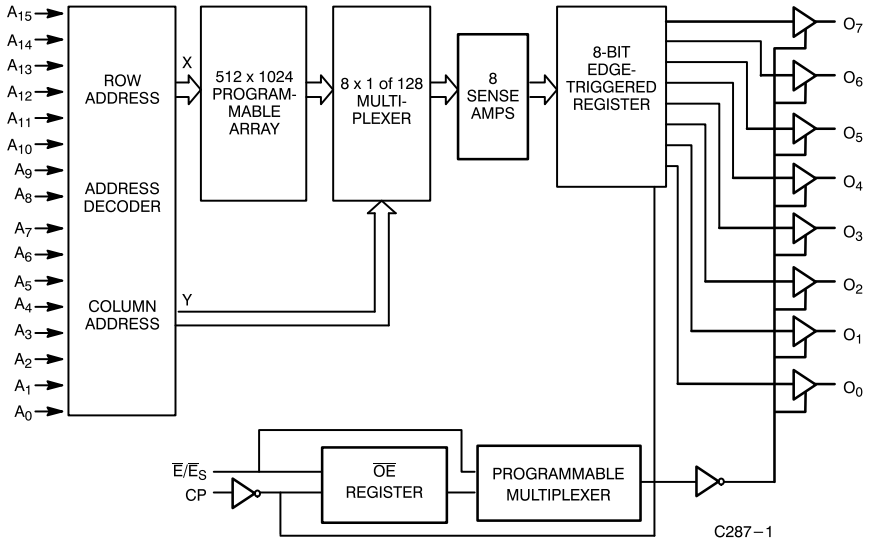
The CY7C287 is a high-performance 64K x 8 CMOS PROM. The CY7C287 is equipped with an output register and an output enable that can be programmed to be synchronous ($\overline{E}_S$) or asynchronous ($\overline{E}$). It is available in a 28-pin, 300-mil package. The address set-up time is 45 ns and the time from clock HIGH to output valid is 15 ns.

The CY7C287 is available in a cerDIP package equipped with an erasure window to provide reprogrammability. When exposed to UV light, the PROM is erased and can be reprogrammed. The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms.

The CY7C287 offers the advantage of low power, superior performance, and programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be 100% tested with each cell being programmed, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

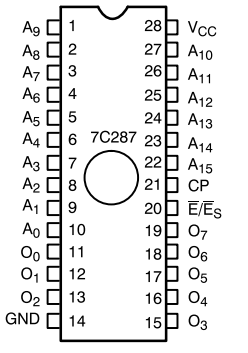
Reading the CY7C287 is accomplished by placing an active LOW signal on $\overline{E}/\overline{E}_S$. The contents of the memory location addressed by the address lines (A_0 – A_{15}) will become available on the output lines (O_0 – O_7) on the next rising of CP.

Logic Block Diagram



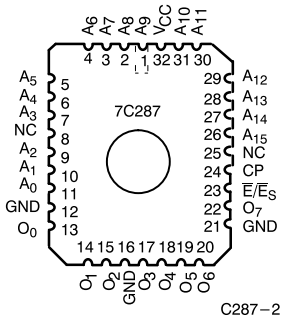
Pin Configurations

CerDIP
Top View



C287–3

LCC/PLCC
Top View



C287–2

Selection Guide

		7C287−45	7C287−55	7C287−65
Maximum Set-Up Time (ns)		45	55	65
Maximum Clock to Output (ns)		15	20	25
Maximum Operating Current (mA)	Com'l	120	120	120
	Mil		150	150

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

DC Program Voltage 13.0V

UV Exposure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015.2)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[1]	−40°C to +85°C	5V ± 10%
Military[2]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7C287−45 Min.	7C287−45 Max.	7C287−55 Min.	7C287−55 Max.	7C287−65 Min.	7C287−65 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA	Com'l		0.4		0.4		0.4	V
		V_{CC} = Min., I_{OL} = 6.0 mA	Mil				0.4		0.4	
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for Inputs		2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for Inputs			0.8		0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	−10	+10	µA
V_{CD}	Input Diode Clamp Voltage			Note 4						
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		−40	+40	−40	+40	−40	+40	µA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND[5]		−20	−90	−20	−90	−20	−90	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		120		120		120	mA
			Mil				150		150	
V_{PP}	Programming Supply Voltage			12	13	12	13	12	13	V
I_{PP}	Programming Supply Current				50		50		50	mA
V_{IHP}	Input HIGH Programming Voltage			3.0		3.0		3.0		V
V_{ILP}	Input LOW Programming Voltage				0.4		0.4		0.4	V

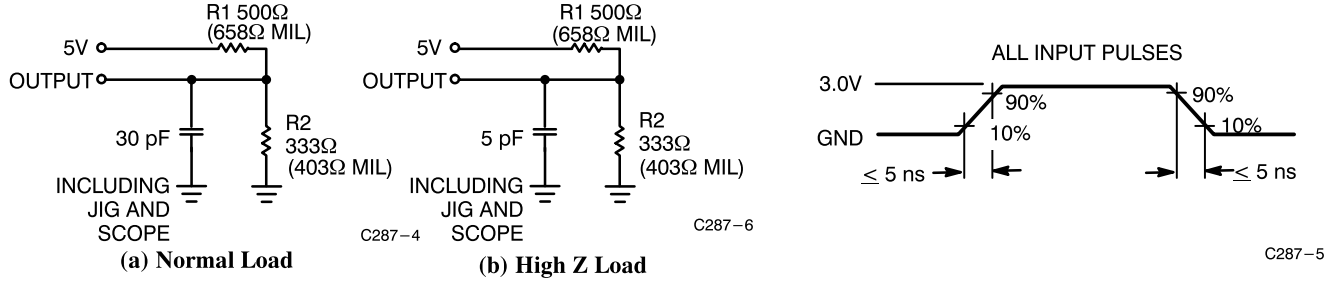
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

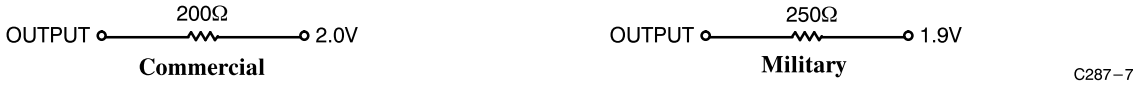
Notes:

1. Contact a Cypress representative for industrial temperature range specifications.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. See Introduction to CMOS PROMs for general information on testing.
5. Short circuit test should not exceed 30 seconds.

AC Test Loads and Waveform[4]



Equivalent to: THÉVENIN EQUIVALENT

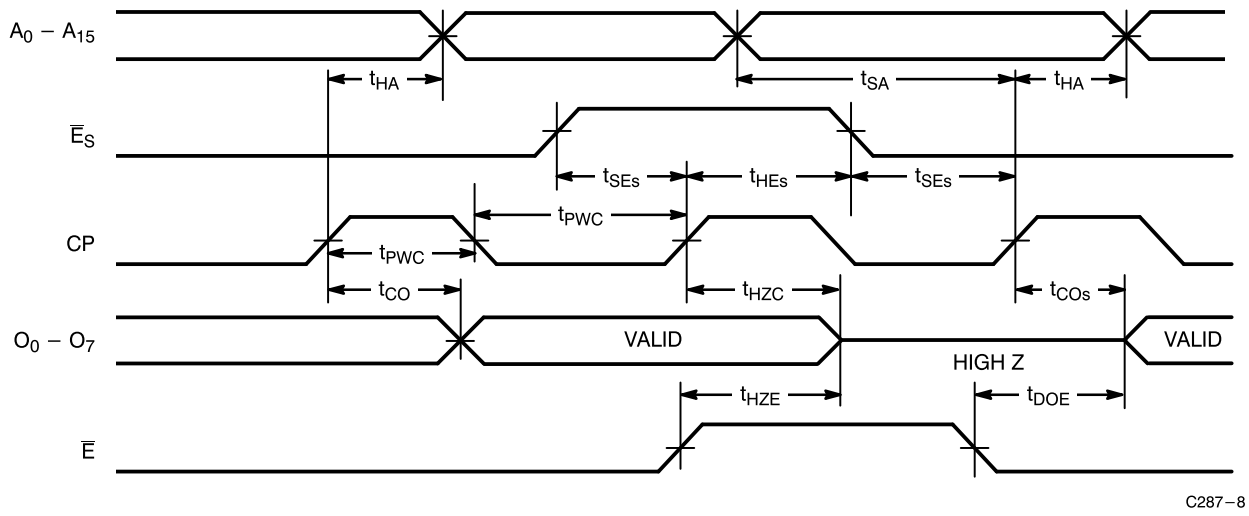


Switching Characteristics Over the Operating Range[3, 4]

Parameter	Description	7C287–45		7C287–55		7C287–65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{SA}	Address Set-Up to Clock HIGH	45		55		65		ns
t_{HA}	Address Hold from Clock HIGH	0		0		0		ns
t_{CO}	Clock HIGH to Output Valid		15		20		25	ns
t_{HZE}	Output High Z from $\overline{E}$		15		20		25	ns
t_{DOE}	Output Valid from $\overline{E}$		15		20		25	ns
t_{PWC}	Clock Pulse Width	15		20		25		ns
t_{SEs}[6]	$\overline{E}_S$ Set-Up to Clock HIGH	12		15		18		ns
t_{HEs}[6]	$\overline{E}_S$ Hold from Clock HIGH	5		8		10		ns
t_{HZC}[6]	Output High Z from CLK/$\overline{E}_S$		20		25		30	ns
t_{COs}[6]	Output Valid from CLK/$\overline{E}_S$		20		25		30	ns

Note:
6. Parameters with synchronous $\overline{E}_S$ option.

Switching Waveform



Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the CY7C287 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The CY7C287 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. CY7C287 Mode Selection

	Pin Function[7]				
Mode: Read or Output Disable	**CP**	**A_{14}**	**$\overline{E}$, $\overline{E}_S$**	**A_{15}**	**$O_7 - O_0$**
Synchronous Read	V_{IL}/V_{IH}	A_{14}	V_{IL}	A_{15}	$O_7 - O_0$
Output Disable – Asynchronous	X	A_{14}	V_{IH}	A_{15}	High Z
Output Disable – Synchronous	V_{IL}/V_{IH}	A_{14}	V_{IH}	A_{15}	High Z
Mode: Other	**$\overline{PGM}$**	**LATCH**	**$\overline{VFY}$**	**V_{PP}**	**$D_7 - D_0$**
Program	V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	$D_7 - D_0$
Program Verify	V_{IHP}	V_{ILP}	V_{ILP}	V_{PP}	$O_7 - O_0$
Program Inhibit	V_{IHP}	V_{ILP}	V_{IHP}	V_{PP}	High Z
Blank Check	V_{IHP}	V_{ILP}	V_{ILP}	V_{PP}	Zeros

Note:
7. X = "don't care" but not to exceed V_{CC} ±5%. X can be V_{IL} ir V_{IH}.

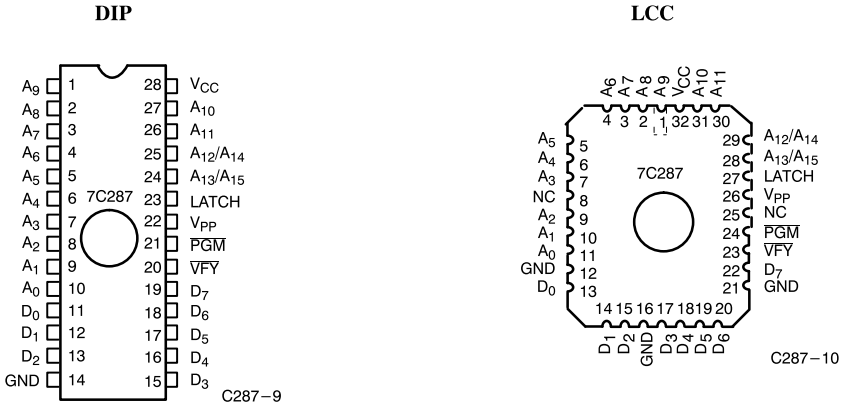


Figure 1. Programming Pinouts

Architecture Configuration Bits

Architecture Bit	Device	Architecture Verify D_0		Function
$\overline{E}/\overline{E}_S$	7C287	D_0	0 = Erased	Asynchronous Output Enable (Pin 20 = $\overline{E}$)
			1 = PGMED	Synchronous Output Enable (Pin 20 = $\overline{E}_S$)

Bit Map

Programmer Address (Hex.)	RAM Data
0000 . . FFFF 10000	Data . . Data Control Byte

Architecture Byte (10000H)

D_7 D_0

C_7 C_6 C_5 C_4 C_3 C_2 C_1 C_0

Ordering Information[8]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
45	CY7C287−45JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C287−45PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C287−45WC	W22	28-Lead (300-Mil) Windowed CerDIP	
55	CY7C287−55JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C287−55PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C287−55WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C287−55DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C287−55LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C287−55QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C287−55WMB	W22	28-Lead (300-Mil) Windowed CerDIP	
65	CY7C287−65JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C287−65PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C287−65WC	W22	28-Lead (300-Mil) Windowed CerDIP	
	CY7C287−65DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C287−65LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY7C287−65QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY7C287−65WMB	W22	28-Lead (300-Mil) Windowed CerDIP	

Note:
8. Most of these products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{SA}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
t_{PWC}	7, 8, 9, 10, 11

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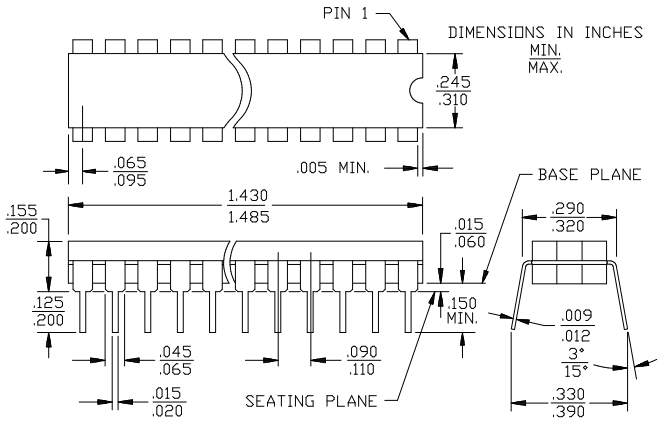
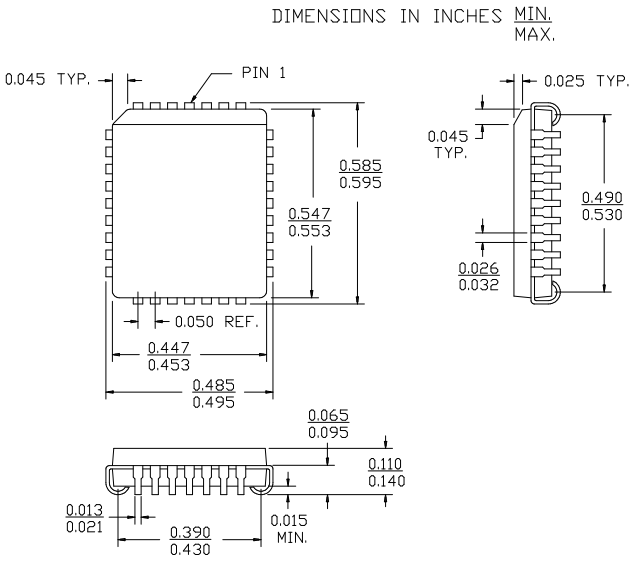
Package Diagrams

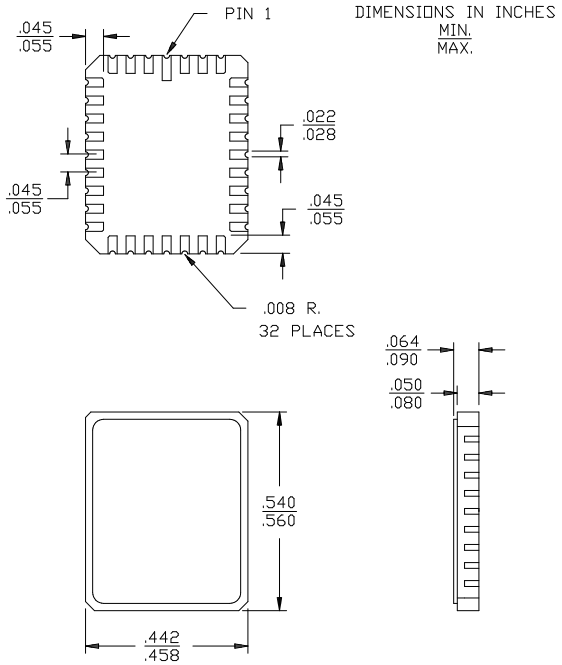
28-Lead (300-Mil) CerDIP D22
MIL−STD−1835 D−15 Config. A



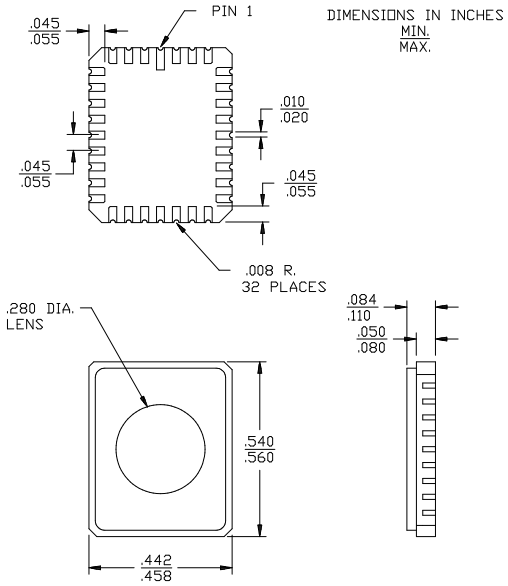
32-Lead Plastic Leaded Chip Carrier J65



32-Pin Rectangular Leadless Chip Carrier L55
MIL−STD−1835 C−12

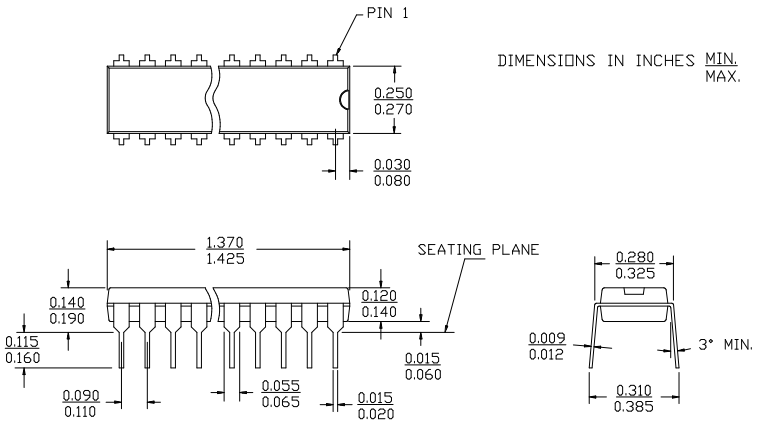


32-Pin Windowed Rectangular Leadless Chip Carrier Q55
MIL−STD−1835 C−12



Package Diagrams (continued)

28-Lead (300-Mil) Molded DIP P21



28-Lead (300-Mil) Windowed CerDIP W22

MIL−STD−1835 D−15 Config. A