Interfacing the CY7C276 High-Speed PROM to the AT&T, AD, Motorola, and TI DSPs

Introduction

Digital signal processors (DSPs) have typically required two external storage devices—a relatively slow PROM (Programmable Read Only Memory) for non-volatile code storage, and an SRAM (Static Random Access Memory), faster than the PROM, from which to run the code. The reason for this is that PROM access times are typically too slow to meet the requirements of the DSP cycle times.

The Cypress CY7C276 is a 16K x 16 UV-erasable PROM that can meet the fast cycle time requirements of a DSP design. It can help reduce component count and cost by eliminating the need for SRAM. If the goal is to eventually place the code in the internal Mask ROM (MROM) of the DSP, (which exists on the AT&T, Motorola and TI devices) then the CY7C276 can be utilized for prototyping until the code is completely debugged. This can save the expense of going to MROM prematurely.

This application note discusses how to use the CY7C276 PROM as program memory for various DSPs. It will cover the topic of interfacing the CY7C276 high-speed PROM to some of today's most popular DSPs for program memory only. Data memory storage is typically done with SRAM and its interface is not included in this application note. The AT&T DSP1616, Analog Devices ADSP 2100A, Motorola DSP56000 and TI TMS320C5x family of devices are discussed. Also included is a detailed description of the CY7C276 (including architecture, programming options, and signal descriptions) and brief descriptions of the DSPs (architectures, signals and timing requirements). For ease of explanation, only one example from each product family is included. The other devices in each product family are similar and are left as an exercise for the reader. Detailed timing calculations that show code sizes up to 16K words in depth are included in the examples. Finally, a table is provided to help summarize the analysis.

An Introduction to the CY7C276

The CY7C276 is a 16K x 16 asynchronous UV-erasable PROM with an access time of 25 ns. There are three polarity-programmable chip selects (CS[2:0]), which provide on-chip decoding of up to eight banks of PROM for a total of 256 Kbytes of PROM. The polarity of the asynchronous output enable (OE) pin is also user programmable. The CY7C276 provides a 16-bit-wide output, thus halving the number of PROMs required when interfacing to 16-bit or wider DSPs. With an access time of 25 ns, the CY7C276 can be used in 40-MHz DSP systems with zero-wait-states.

In all following examples, the CY7C276 is programmed to have all three chip enables (CS[2:0]) and the output enable (OE) active LOW. This is achieved by programming a Hex 0008 in location H4000.

AT&T – DSP1616

The DSP1616 is a 16-bit fixed-point DSP based on the popular DSP1600 core. It is object code upward-compatible with the DSP16, 16A, 16C, and 1610 devices from AT&T.

The DSP1616 can run out of either the 12K 16-bit words of on-chip MROM or external memory of up to 56K 16-bit words. Data memory space can also be accessed externally, although this application note only describes the external program memory interface. *Table 1* shows memory maps for the various configurations of DSP1616. IROM is Internal ROM, EROM is External ROM and RAM1/RAM2 are internal memory locations that are not utilized in this design and are therefore left as "don't cares." Two parameters, LOWPR and EXM, determine which memory map is used. LOWPR controls the address in memory assigned to the RAM1 and RAM2 areas. EXM (EXternal Memory) is an input signal that determines whether the internal ROM (IROM) or the external ROM (EROM) will be addressed in the memory map at location 0.

Initialization

The DSP must be reset after power-up to begin executing code. Reset is administered by asserting the RSTB (Reset Bar) pin LOW. When the RSTB pin is driven HIGH, the DSP1616 comes out of reset and fetches an instruction from location zero of the program space. The physical location of address zero is determined by which memory map is selected. The DSP1616 is configured for external ROM by holding the EXM (External ROM enable) signal HIGH at the rising edge of RSTB. With the LOWPR bit set to 0 at reset, the corresponding memory map selected is Map2 (*Table 1).* This locates EROM at address 0.

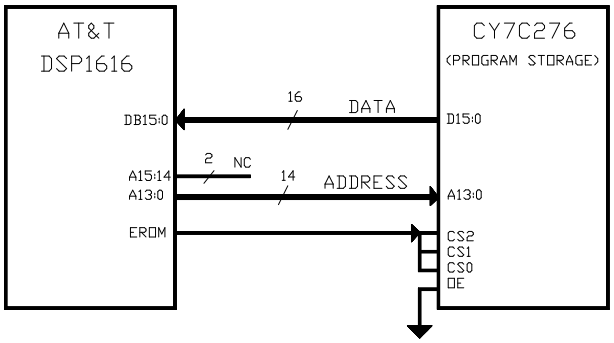

Figure 1. AT&T DSP1616 to PROM Interface

DSP to Memory Interface

The DSP1616 uses the following signals to interface with external memory.

AB[15:0] – Address Bus. Outputs memory and I/O addresses.

DB[15:0] – Data Bus. Used to transfer data to and from the processor.

$\overline{\text{EROM}}$ – (Program address External ROM enable) Access enable for external memory. Active LOW.

The implementation of the DSP to PROM interface is shown in *Figure 1*.

Table 1. DSP1616 Memory Maps

Decimal Address	MAP1 EXM = 0 LOWPR = 0	MAP2 EXM = 1 LOWPR = 0	MAP3 EXM = 0 LOWPR = 1	MAP4 EXM = 1 LOWPR = 1
0	IROM	EROM	RAM1	RAM1
1K			RAM2	RAM2
2K			Reserved	Reserved
8K			IROM	EROM
12K	RAM1	RAM1		
13K	RAM2	RAM2		
14K	Reserved	Reserved		
20K 64K−1	EROM	EROM	EROM	

Timing Notes

The DSP1616 has numerous mask-programmable options for the clock source. It can use a crystal oscillator, or a small signal (TTL, or CMOS level) oscillator. The external source can be supplied by either a crystal or an oscillator. These options are discussed in detail in the AT&T DSP1616 datasheet. The DSP1616 can run at either the same or half the input frequency. The datasheet calls this a 1x or 2x clock, referring to the ratio of the input clock to the processor (internal) clock. *Table 4* notes this as the 1x and 2x clock options respectively.

The calculations for the required access time of the CY7C276 are illustrated below. The timing diagram for this example is shown in *Figure 2*.

$t_{AA}(PROM) = (t_{c(CKO)} - 2) - t_{ASKW(DSP)} - t_{SU(D)R}$

where:

$t_{AA}(PROM)$ = PROM address access time required,

$t_{c(CKO)}$ = DSP CKO cycle time [$t_{c(CKO)}$ − 2 is to compensate for the worst-case EROM cycle time, which would be 2 ns shorter than CKO, as specified in the DSP1616 datasheet]. CKO is the clock out signal from the DSP,

$t_{ASKW}(DSP)$ = Worst-case address valid time from edge of cycle, and

$t_{SU(D)R}$ = Read data set-up time required by DSP before EROM goes HIGH.

Substituting values from a DSP1616 datasheet gives us:

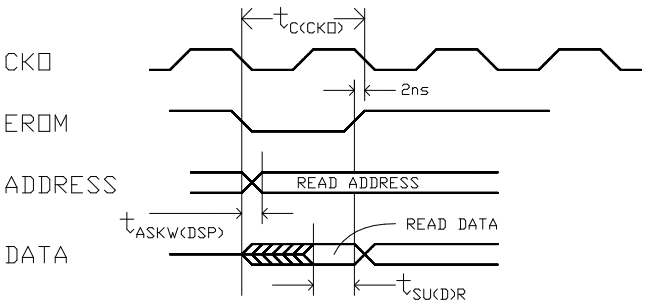

Figure 2. DSP1616 External Program Memory Timing

$t_{AA}(PROM) = (50 \text{ ns} - 2) - 2 \text{ ns} - 17 \text{ ns} = 29 \text{ ns}.$

for a 40-MHz DSP with the 2x input clock option.

Summary

From the above analysis, it can be seen that AT&T's DSP1616 can run code directly out of a CY7C276 at 40 MHz with the 2x input clock option with zero wait states. The CY7C276−25 (25-ns access time) can be used to satisfy this requirement.

Analog Devices − ADSP2100A

The ADSP2100A is a 24-bit fixed-point DSP that utilizes 24-bit instructions. It has a 14-bit address bus that directly addresses 16K 24-bit words externally and is expandable to 32K 24-bit words by using the program memory data access (PDMA) signal as a chip select. This example discusses the memory interface for 16K 24-bit words of program size. There is no on-chip memory for code/data storage. The ADSP2100A is the fastest available 24-bit DSP from Analog Devices that can access external ROM. (As of writing this application note.) It has a maximum clock frequency of 12.5 MHz.

Initialization

The DSP must be reset after power-up to begin executing code. Reset is administered by driving the $\overline{\text{RESET}}$ pin LOW. When the $\overline{\text{RESET}}$ pin is driven HIGH, the ADSP2100A comes out of reset and fetches an instruction from location H0004 of the program space (The first three locations of memory contain the interrupt vector addresses). In the case of the ADSP2100A, where there is no internal memory, the address (H0004) appears on the program memory address (PMA) bus followed by assertion of the program memory select ($\overline{\text{PMS}}$) and program memory read ($\overline{\text{PMRD}}$) signals. The DSP has completed the reset sequence and is now ready to execute code.

DSP to Memory Interface

The ADSP2100A uses the following signals to interface with external memory.

PMA[13:0] − Address Bus. Outputs memory and I/O addresses.

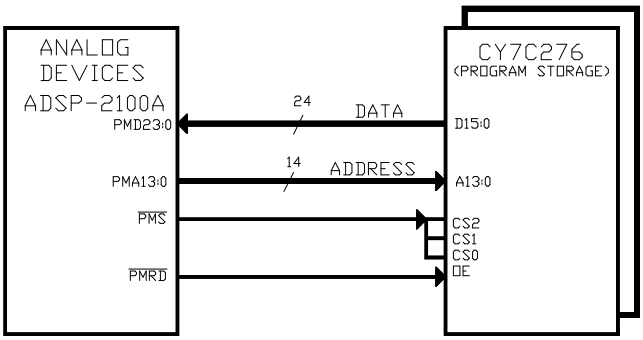

Figure 3. ADSP2100A to PROM Interface

PMD[23:0] − Data Bus. Used to transfer data to and from the processor.

$\overline{PMS}$ − Program Memory Select. Used to access external memory.

$\overline{PMRD}$ − Program Memory Read. Used for external memory output enable.

The implementation of the DSP to PROM interface is shown in *Figure 3*.

Timing Notes

The ADSP2100A datasheet directly specifies the maximum allowable access times to run code directly out of PROM. The timing diagram for this example is shown in *Figure 4*.

The result with the DSP running at a frequency of 12.5 MHz is:

t_{AA}(PROM)max = 32 ns.

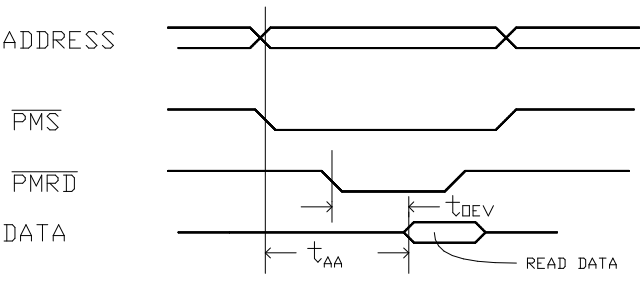

Figure 4. ADSP2100A External Program Memory Timing

where:

t_{AA}(PROM) = PROM address access time required. This is specified in the datasheet as PMA valid to PMD input valid.

Because this device uses the $\overline{PMRD}$ signal to control the OE of the CY7C276, the OE to data valid time must also be calculated. The following was also directly specified in the datasheet as $\overline{PMRD}$ LOW to PMD input valid.

t_{OEV}(PROM)max = 18 ns.

The CY7C276−30 satisfies both of these timing requirements.

Summary

From the above analysis, it can be seen that Analog Devices' ADSP2100A can run code directly out of two CY7C276s with zero wait states at its maximum frequency of 12.5 MHz. The CY7C276−25 or CY7C276−30 (25-ns and 30-ns access times, respectively) can be used to satisfy this requirement.

Motorola − DSP56000

The DSP56000 is a 24-bit general purpose DSP. It has 3.75K x 24-bits of on-chip ROM and can also run from external memory of 64K 24-bit words of program space. *Table 2* shows the memory maps for the various configurations of DSP56000. Mode 0 is the single-chip mode for use with internal ROM only. Mode 1 on the DSP56000 is for test purposes only and should not be invoked. Mode 2 is the normal expanded mode and is identical to Mode 0 except that the reset vector is in a different location. Mode 3 is Development Mode, which disables the internal ROM. All references to program memory space in this mode are directed to external program memory. There are two pins (MODA and MODB) that are sampled at the end of reset to determine which memory map is used.

Initialization

The DSP must be reset after power-up to begin executing code. Reset is administered by driving the $\overline{RESET}$ pin LOW. When the $\overline{RESET}$ pin is driven HIGH, the DSP56000 comes out of reset and

fetches an instruction from the reset vector location of the program space. The physical location of the reset vector is determined by which memory map is selected. If MODE 0 or 3 is selected, the reset vector is at location H0000 (location 0). If MODE 2 is selected, the reset vector is at location HE000. The DSP56000 is configured for external ROM by setting MODA and MODB HIGH at the rising edge of $\overline{\text{RESET}}$. The state of MODA and MODB will determine which memory map is selected for use (see *Table 2*). This example will use MODE 3 (Development Mode).

So, for MODE3, DSP56000 will start executing code from location zero of the external memory after reset is complete. All 64K words of external memory, except the first 64 locations (used for interrupts), are available for program storage. Location H0000 contains the reset vector which holds the programs starting address. This example will use two CY7C276 16K x 16 PROMs to achieve the 24-bit-wide program memory bus that is required. The upper eight bits of the PROM will not be used.

DSP to Memory Interface

The DSP56000 uses the following signals to interface with external memory.

A[13:0] – Address Bus. Outputs memory and I/O addresses.

D[23:0] – Data Bus. Used to transfer data to and from the processor.

$\overline{\text{PS}}$ – Program Memory Select. Used to access external memory.

$\overline{\text{RD}}$ – Read Select. Used for external memory output enable.

The implementation of the DSP to PROM interface is shown in *Figure 5*.

Timing Notes

The DSP56000 takes two external clock cycles for a read operation. The address becomes available at about the midpoint of the first cycle referenced from the falling edge of clock. The data is read into the DSP at the middle of the second cycle or the second rising edge of clock (see *Figure 6*). This actually works to the PROM's advantage by lengthening the required access time.

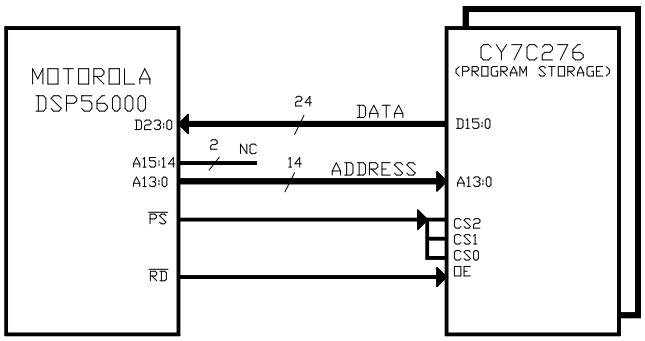

Figure 5. Motorola DSP56000 to PROM Interface

Table 2. DSP56000 Memory Maps

Decimal Address	MODE 0 MB = 0 MA = 0 Internal ROM Internal Reset	MODE 1* MB = 0 MA = 1 TEST MODE DO NOT USE	MODE 2 MB = 1 MA = 0 Internal ROM External Reset	MODE 3 MB = 1 MA = 1 No Int. ROM External Reset
0	Reset			Reset
3839 (H0EFF)	INTERNAL ROM		INTERNAL ROM	
3840	EXTERNAL		EXTERNAL	EXTERNAL
60K			Reset	
64K–1				

* Mode 1 is for test purposes only on the DSP56000 and should not be invoked by the user.

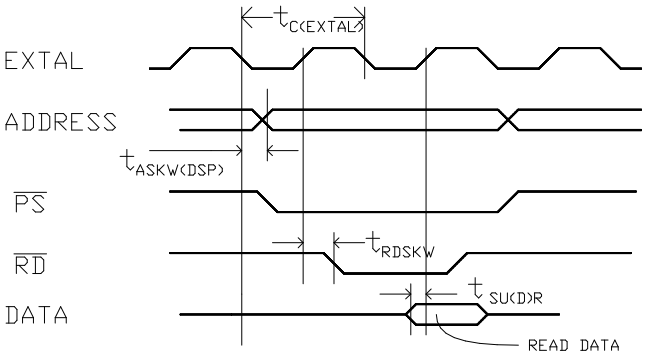

Figure 6. Motorola DSP56000 External Program Memory Timing

The calculations for the required access time of the CY7C276 are shown below. The timing diagram for this example is shown in *Figure 6*.

$t_{AA}(PROM)max = t_{c+} - t_{ASKW}(DSP) - t_{SU(D)R}$

where:

$t_{AA}(PROM)$ = PROM address access time required,

t_{c+} = DSP CLOCK IN cycle time x 1.5 (due to data read into DSP occurring at midpoint of second external clock cycle),

$t_{ASKW}(DSP)$ = Worst case address valid from edge of cycle, and

$t_{SU(D)R}$ = Read data set-up time before end of cycle.

This device uses the $\overline{RD}$ signal to control the OE of the CY7C276. Therefore, the OE access time must also be calculated. The following equation is for calculating the maximum allowable OE time of the CY7C276.

$t_{OEV}(PROM)max = t_{c(EXTAL)} - t_{RDSKW} - t_{SU(D)R}$

where:

$t_{c(EXTAL)}$ = clock cycle,

$t_{RDSKW}(DSP)$ = Worst case $\overline{RD}$ valid from edge of cycle, and

$t_{SU(D)R}$ = Read data set-up time before end of cycle.

The result with the DSP running at a frequency of 33 MHz is:

$t_{AA}(PROM)max = (30 \times 1.5)\ ns - 19\ ns - 0\ ns$
$= 45\ ns - 19\ ns$
$= 26\ ns.$

$t_{OEV}(PROM)max = 30ns - 16ns - 0ns = 14ns.$

Summary

Based on the above analysis, it can be seen that Motorola's DSP56000 can run code directly out of a CY7C276 with zero-wait-states at its maximum frequency of 33 MHz. The CY7C276−25 (25-ns access time) can be used to satisfy this requirement.

Texas Instruments − TMS320C5X

The TMS320C5X devices are a family of 16-bit fixed-point DSPs based on the older TMS320C25 CPU core. Significant modifications were added to improve performance. These devices are capable of running at twice the speed of the 'C2x family and are source-code upward compatible with all previous fixed-point DSPs from TI.

There are three devices in the 'C5x family, the 'C50, 'C51 and 'C53. They have 2K, 8K and 16K words of on-chip ROM, respectively. All three devices can run out of external ROM of up to 64K 16-bit words. All 64K words of external memory are available for program storage. *Table 3* shows the memory map for the TMS320C50 as an example. The SARAM is 9K words of program/data Single-Access RAM. This is memory that can only be read or written in a single machine cycle. It can reside on-chip or externally depending on the setting of the RAM bit in the PMST register. The DARAM is 1056 words of Dual-Access data RAM. It can be read from or written to in the same cycle. The DARAM can reside on-chip or externally depending on the setting of the CNF bit on the PMST register. The map in *Table 3* gives an example of the use of these two sections of memory.

Initialization

The DSP must be reset after power-up to begin executing code. Reset is administered by asserting the $\overline{RS}$ pin LOW. When the $\overline{RS}$ pin is driven HIGH,

the TMS320C5x comes out of reset and fetches an instruction from location 0. Location 0 (either on-chip or externally) contains the reset vector. The TMS320C5x is configured for external memory by holding the MP/$\overline{MC}$ pin HIGH at the rising edge of $\overline{RS}$.

Table 3. TMS320C50 Memory Maps

Decimal Address	'C50 MAP 1 MP/$\overline{MC}$ = 1 Internal	'C50 MAP 2 MP/$\overline{MC}$ = 0 External
0	Interrupts & Reserved (On-Chip)	Interrupts & Reserved (External)
48	On-Chip ROM	External
2K	On-Chip SARAM (RAM=1)	SARAM (RAM=0)
11K	External	External
63.5K 64K−1	On-Chip DARAM B0 (CNF=1)	DARAM External (CNF=0)

DSP to Memory Interface

The TMS320C5x uses the following signals to interface with external memory.

A[15:0] − Address Bus. Outputs memory and I/O addresses.

D[15:0] − Data Bus. Used to transfer data to and from the processor.

$\overline{PS}$ − Program Memory Select. Used to access external memory.

$\overline{RD}$ − Read Select. Used for external memory output enable.

The implementation of the DSP to PROM interface is shown in *Figure 7*.

Timing Notes

The TMS320C5x can use either its internal oscillator or an external frequency source for a clock. The external source can either be a crystal or an oscillator. These options are discussed in detail in the TI User's Guide for the TMS320C5x. The TMS320C5x can run at either the same or half the input frequency. This means that the internal machine cycle and, subsequently, external accesses, can cycle at the same or one-half times the external frequency. The table at the end of this document notes this as the ÷1 and ÷2 clock options respectively.

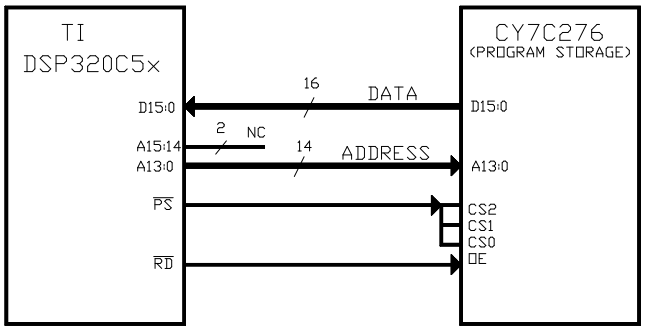

Figure 7. TMS320C5x to PROM Interface

The calculations for the required access time of the CY7C276 are illustrated below. The timing diagram for this example is shown in *Figure 8*.

$t_{AA}(PROM) = t_{c(CO)} - t_{ASKW}(DSP) - t_{SU(D)R}$

where:

$t_{AA}(PROM)$ = PROM address access time,

$t_{c(CO)}$ = DSP CLKOUT1 cycle time,

$t_{ASKW}(DSP)$ = Worst case address valid from edge of cycle, and

$t_{SU(D)R}$ = Read data set-up time before $\overline{RD}$ goes HIGH.

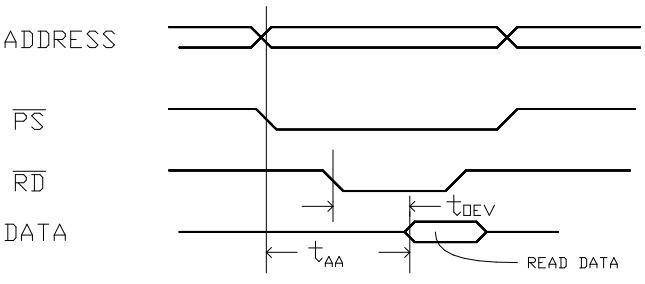

Figure 8. TMS320C5x External Program Memory Timing

The result with a frequency of 40 MHz and using the divide-by-two clock option the result is:

t_{AA}('276)max = 48.8 ns − 2 ns − 10 ns = 36.8 ns.

Summary

Based on the above analysis, it can be seen that TI's TMS320C5x series of DSPs can run code directly out of a CY7C276 at 40 MHz with zero-wait-states. The CY7C276−25 or CY7C276−30 (25-ns and 30-ns access times, respectively) can be used to satisfy this requirement.

Table 4 below has been provided to give a quick synopsis of the processors covered in this application note. It provides a quick cross reference of the CY7C276 PROM access times to DSP clock speeds and the number of wait states required.

Summary

These examples show how effectively the CY7C276 PROM can be used for executing code in DSP applications. The need for more costly SRAM is eliminated. There is no additional logic required to interface the PROM to the DSP thereby reducing pin count and cost in the design. As *Table 4* illustrates, most of the DSP speed grades can run code directly out of the CY7C276 with zero-wait-states.

Table 4. Wait State Requirements

DSP PART NUMBER	DSP Frequency and Clock Option If Applicable	# of Wait States Required for each PROM		
		CY7C276−25	CY7C276−30	CY7C276−35
AT&T DSP1616	20 MHz w/1x clock	0	1	1
	40 MHz w/2x clock	0	1	1
	20 MHz w/2x clock	0	0	0
ADSP2100A	12.5 MHz	0	0	1
	10.24 MHz	0	0	0
DSP56000	33 MHz	0	1	1
	27 MHz	0	0	0
	20.5 MHz	0	0	0
TMS320C5X	57 MHz with ÷1 clock option	2	3	3
	40 MHz with ÷1 clock option	1	2	2
	57 MHz with ÷2 clock option	1	1	1
	40 MHz with ÷2 clock option	0	0	1