Using the CY27H010 with the Rockwell V.FAST Chipset

The purpose of this application note is to describe how to use the Cypress CY27H010 1-megabit PROM with the Rockwell V.FAST chipset to create a high-speed fax/modem. A system block diagram and timing analysis are included.

Traditionally, PROMs have been ideal for non-volatile code storage in embedded systems such as modems, yet have been unable to provide the speed necessary to meet system requirements. In order to solve this performance bottleneck, designers typically download code from the slow PROM into a fast, yet expensive SRAM. Usually, this transfer takes place during system boot-up and is transparent to the user. Once in SRAM, code can be run much faster, usually with 0 wait states. The obvious trade-offs for this added performance are the cost of the SRAM, board area, and design complexity.

The introduction of the fast Cypress CY27H010 1-megabit (128Kx8) PROM has eliminated the need for this compromise in many systems. The CY27H010 delivers the performance required to run code at full speed directly out of the PROM. Not only will this simplify the design, it will also lower the system cost and board area. In addition to being fast enough for most high-speed applications, the CY27H010 is also large enough to satisfy most code storage requirements. These two factors are demonstrated below as the CY27H010 is used with the Rockwell V.FAST chipset at full speed, with 0 wait states.

The Rockwell V.FAST modem device set consists of three separate devices: (1) the L39 Micro Controller unit (MCU), which performs all of the command processing and host interface operations, (2) the Modem Data Pump (MDP), which can operate as either a data modem at up to 28.8 Kbps, or a fax modem up to 14.4 Kbps, and (3) the optional Compression Expansion Processor (CEP), which can increase system performance by performing dedicated compression and expansion functions in V.42 bis or MNP 5 modes. The CY27H010 provides the code storage for the MCU and is independent of the configuration (serial or parallel) or whether the CEP is being used. An additional SRAM is required to provide scratch pad memory for the MCU, but that topic is beyond the scope of this application note. If used, the CEP requires an additional SRAM and PROM for code storage and scratch pad memory. These additional devices are not involved in this discussion.

Typically, when designing with a Micro Controller like the L39, the engineer must become familiar with all of the various modes, functions, and registers of the device. This is essential in order to set the numerous registers that establish the appropriate functionality. An example of the variables that need to be set are: number of wait states when accessing external PROM, polarity of certain signals, ...etc. This tedious process has been simplified when using the Rockwell V.FAST chipset. Rockwell provides the firmware necessary to properly configure the MCU. A PC-based utility program is available that allows designers to modify the base configuration in order to suit their particular requirements. When the default settings are used, all of the required parameters are established that affect the MCU-PROM interface on the expansion bus. These parameters are: (1) 1X internal clock frequency (20.5-MHz external and internal, this provides a

48.1-ns cycle time), (2) establishing the functionality of the $\overline{\text{ROMSEL}}$ output on Port B, bit 2, and (3) 0 wait state operation when accessing the expansion bus.

One requirement placed on the hardware design is to enable or disable the 8 KB of on-chip ROM. The on-chip ROM is mask programmable and therefore is of little use during system development or when a large program is required. Once the code has solidified, this on-chip ROM can be used for code storage, provided the size of the code is less than 8 KB. This on-chip ROM can be disabled by grounding the TST pin on the MCU. By doing so, the device will automatically look to the expansion bus for ROM accesses and during the boot sequence.

Once configured, the MCU uses Port B, bit 2 as the $\overline{\text{ROMSEL}}$ output. This signal is used to select the appropriate external device, which in this case is the PROM. This signal should be tied directly to the $\overline{\text{CS}}$ input of the PROM. If multiple PROMs were being used, additional $\overline{\text{ROMSEL}}$ lines would be generated in order to select the correct device. The MCU also generates a $\overline{\text{READ}}$ signal that is strobed LOW during external read cycles. This signal should be connected to the $\overline{\text{OE}}$ of the CY27H010. By using the $\overline{\text{OE}}$ pin we are able to take advantage of the fast t_{DOE} in order to satisfy system timing. The MCU-PROM interface is shown in *Figure 1*.

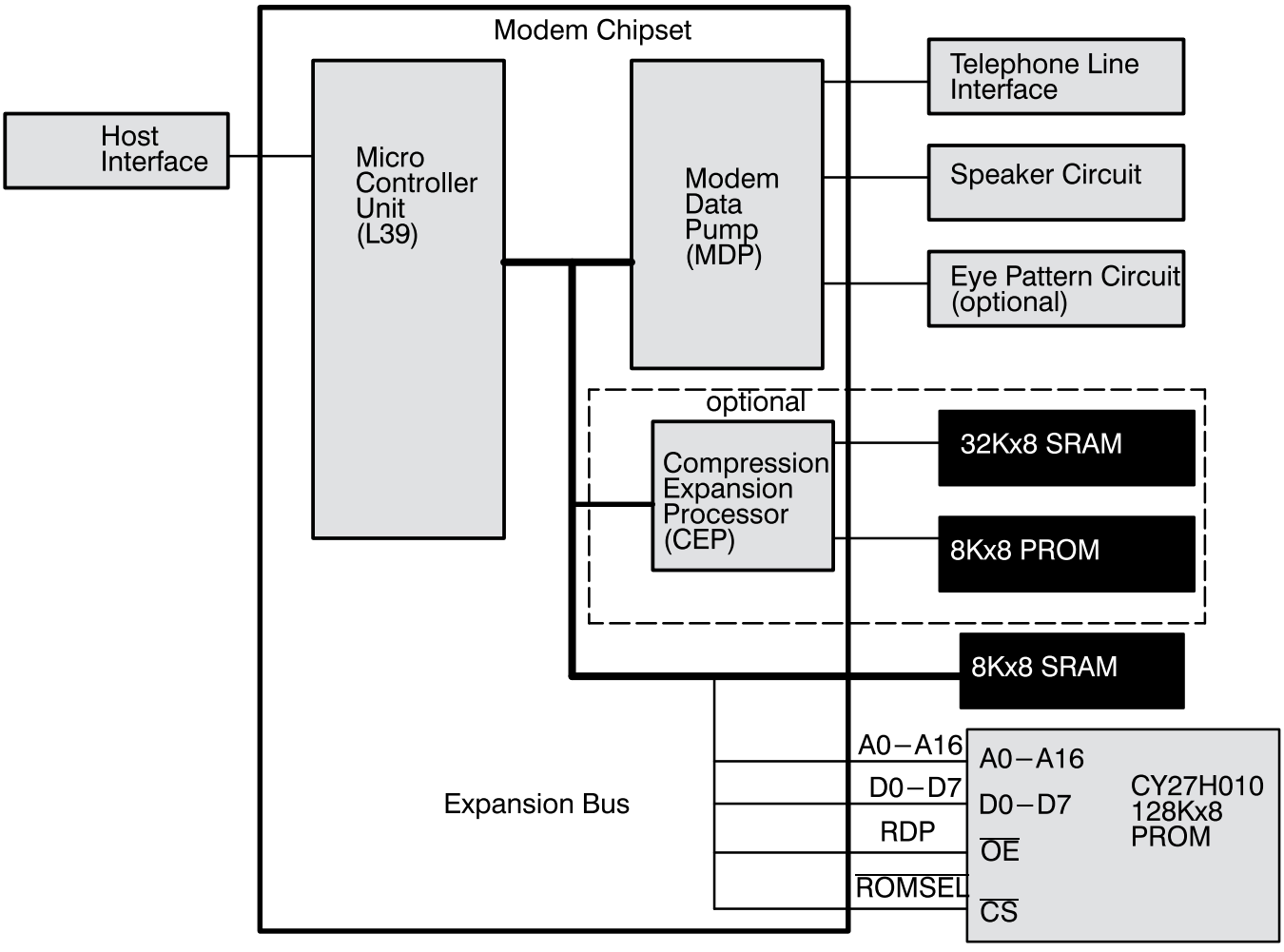

Figure 1. Rockwell V.FAST Modem Block Diagram

Timing Analysis

A basic read on the expansion bus is shown in *Figure 2*. As can be seen in the diagram, the address, $\overline{\text{ROMSEL}}$, and $\overline{\text{READ}}$ signals are generated from one falling edge of the clock, and the data is captured by the MCU on the next falling edge. A/C timing must now be verified. Although the critical path is through t_{DOE}, t_{AA} and t_{ACE} must be verified as well. All timing specifications were taken directly out of the L39 MCU technical manual.

t_{AA} (required) $= t_{CYC} - t_{AS} - t_{RDS}$
$= 48.1 - 12.0 - 4.5$
$= 31.6$ ns (t_{AA} max. for CY27H010−25 is 25 ns!)

t_{ACE} (required) $= t_{CYC} - t_{AS} - t_{RDS}$
$= 48.1 - 12.0 - 4.5$
$= 31.6$ ns (t_{ACE} max. for CY27H010−25 is 30 ns!)

t_{DOE} (required) $= t_{RW} - t_{RDS}$
$= 24.6 - 4.5$
$= 20.1$ ns (t_{DOE} max. for CY27H010−25 is 15 ns!)

All of the A/C requirements shown above can be satisfied with a CY27H010−25 device.

Conclusion

With the firmware provided by Rockwell, the functional interface between the MCU and the PROM has been greatly simplified. In addition, the timing provided in the Rockwell has made the A/C analysis straight forward. After comparing the required A/C numbers to those published in the CY27H010 data sheet, it is apparent that a CY27H010−25 device is able to provide the speed required by the Rockwell V.FAST chipset to run code directly out of PROM with 0 wait states.

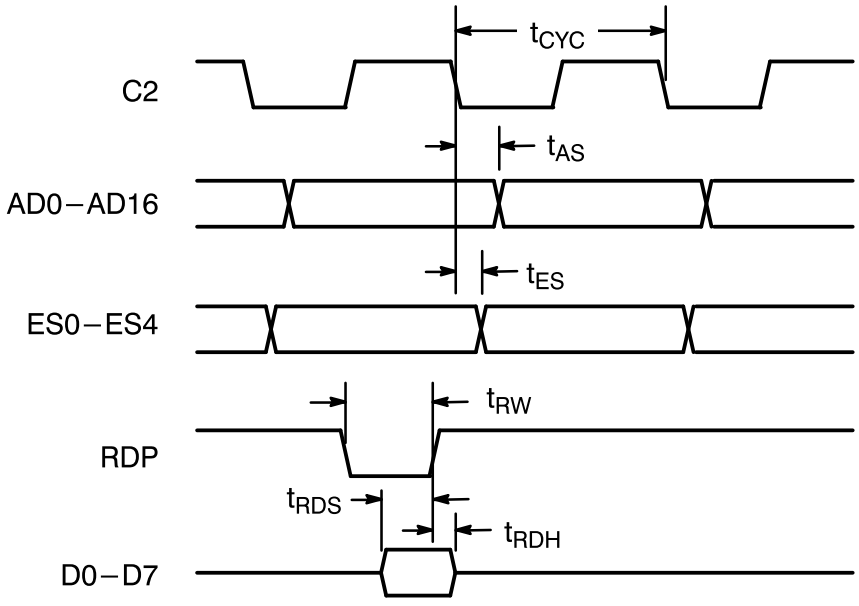

Figure 2. Expansion Bus Read Waveform